

EUROSOI-ULIS 2017

Third Joint International EUROSOI-ULIS Conference on SOI and Ultimate Integration on Silicon

April 3-5, 2017 - Athens, Greece

The third joint **EUROSOI-ULIS** event will be hosted by the Institute of Nanoscience & Nanotechnology of NCSR "Demokritos" in Athens, Greece. The focus of the sessions is on SOI technology and advanced nanoscale devices. The organizing committee invites scientists and engineers working in the above fields to actively participate by submitting high quality papers. Original **2-page abstracts** with illustrations will be accepted for review in pdf format. The **template** is available at the conference website: <u>eurosoi-ulis2017.inn.demokritos.gr</u>

The deadline for abstract submission is December 20th, 2016.

The accepted abstracts will be published in a **Proceedings book** with an ISBN.

A **4-page follow-up paper** delivered before April 3, 2016 will be published in **IEEE Xplore Digital Library**. The authors of the best papers will be invited to submit a longer version for publication in a special issue of **Solid-State Electronics**. A best paper award will be attributed to the best paper by the SINANO institute.



Papers in the following areas are solicited:

- · Advanced SOI materials and wafers. Physical mechanisms and innovative SOI-like devices.
- New channel materials for CMOS: strained Si, strained SOI, SiGe, GeOI, III-V and high mobility materials on insulator; carbon nanotubes; graphene and other two-dimensional materials.
- Properties of ultra-thin films and buried oxides, defects, interface quality. Thin gate dielectrics: high-k materials for switches and memory.
- Nanometer scale devices: technology, characterization techniques and evaluation metrics for high performance, low power, low standby power, high frequency and memory applications.
- Alternative transistor architectures including FDSOI, DGSOI, FinFET, MuGFET, vertical MOSFET, Nanowires, FeFET and Tunnel FET, MEMS/NEMS, Beyond-CMOS nanoelectronic devices.
- New functionalities in silicon-compatible nanostructures and innovative devices representing the More than Moore domain, nanoelectronic sensors, biosensor devices, energy harvesting devices, RF devices, imagers, etc.
- CMOS scaling perspectives; device/circuit level performance evaluation; switches and memory scaling. Three-dimensional integration of devices and circuits, heterogeneous integration.
- Transport phenomena, compact modeling, device simulation, front- and back-end process simulation.
- Advanced test structures and characterization techniques, parameter extraction, reliability and variability assessment techniques for new materials and novel devices.

Conference Chair: Androula Nassiopoulou

Technical Program Chair: Francis Balestra







