2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (ULIS)

April 3-5, 2017 - Athens, Greece

PROGRAM

SUNDAY, APRIL 2, 2017

16^{00} – 19^{00} **Registration**

Divani Caravel Hotel,

Vassileos Alexandrou 2,

16121 Athens - Greece

MONDAY, APRIL 3, 2017

09^{00} – 09^{30} ***Welcome***

Conference Chairperson

Session 1: Nanoscale FETs

Session Chairs: Androula Nassiopoulou, Francis Balestra

09^{30} – 10^{00} **Transistor architecture and channel materials for nanoscale FET**

Dr. Anda Mocuta **(Invited)**

IMEC, Leuven, Belgium

10^{00} – 10^{15} **Modeling and Design Considerations for Negative Capacitance Field-Effect Transistors**

Michael Hoffmann, Milan Pešić, Stefan Slesazeck, Uwe Schroeder, Thomas Mikolajick

NaMLab gGmbH, Noethnitzer Str. 64, D-01187 Dresden, Germany

10^{15} – 10^{30} **On quantum effects and Low Frequency Noise spectroscopy in Si Gate-All-Around Nanowire MOSFETs at cryogenic temperatures**

D. Boudier[1], B. Cretu[1], E. Simoen[2], A. Veloso[2] and N. Collaert[2]

[1]Normandie Univ, UNICAEN, ENSICAEN, CNRS, GREYC, 14000 Caen, France, [2]Imec, Kapeldreef 75, B-3001 Leuven, Belgium

10^{30} – 10^{45} **First SOI Tunnel FETs with Low-Temperature Process**

C. Diaz Llorente[1], C. Le Royer[1], C-M. V. Lu[1], P. Batude[1], C. Fenouillet-Beranger[1], S. Martinie[1], F. Allain[1], S. Cristoloveanu[2], G. Ghibaudo[2], and M. Vinet[1]

[1] CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France,
[2] IMEP-LAHC, INP-Grenoble, MINATEC campus, 38016 Grenoble, France

10^{45} – 11^{00} **Impact of strain and traps on optimized n- and p-type TFETs**

M. Visciarelli, E. Gnani, A. Gnudi, S. Reggiani, G. Baccarani

ARCES and DEI, University of Bologna, Bologna 40136, Italy

11^{00} – 11^{30} ***Coffee Break***

Session 2: More than Moore devices and applications, Heterogeneous Integration, Other

Session Chairs: Lars-Erik Wernersson, Luca Selmi

11^{30} – 12^{00} **Micro and Nano transducers for autonomous sensing applications**

Dr. Cosmin Roman **(Invited)**

ETH Zurich

12^{00} – 12^{15} **Out-of-Equilibrium Body Potential Measurements in Ψ-MOSFET for Biosensing**

Licinius Benea[1], Marylline Bawedin[1], Cécile Delacour[2], Sorin Cristoloveanu[1], Irina Ionica[1]

[1]IMEP-LAHC, Minatec, Grenoble INP, Univ. Grenoble Alpes, CNRS, 38016 Grenoble, France,
[2] Néel Inst., CNRS, 38042 Grenoble, France, France

12^{15} – 12^{30} **Electrical Characterization of Percolating Si-Nanonet FET for sensing applications**

T. Cazimajou[1], M. Legallais[1,2], M.Mouis[1], C. Ternon[2,3], B.Salem[3],G. Ghibaudo[1]

[1]Univ Grenoble Alpes, CNRS, Grenoble INP, IMEP-LaHC, F 38000 Grenoble, France,
[2]Univ Grenoble Alpes, CNRS, Grenoble INP, LMGP, F 38000 Grenoble, France,
[3]Univ Grenoble Alpes, CNRS, Grenoble INP, LTM, F 38000 Grenoble, France

12^{30} – 12^{45} **Influence of Free Radical Surface Activation on Si/SiC Heterogeneous Integration by Direct Wafer Bonding at Room Temperature**

P. Torchia[1], P. Pampili[1], J. O'Connell[2], J. O'Brien[1], M. White[1], M. Schmidt[1], B. Sheehan[1], F. Waldron[1], J. D. Holmes[2], S. Monaghan [1], R. Duffy[1], T. Trajkovic[3], V. Kilchytska[4], P. Gammon[5], K. Cherkaoui[1], P. K. Hurley[1], and F. Gity[1]

(1) Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland,
(2) Chemistry Department, University College Cork, Cork, Ireland,
(3) Cambridge Microelectronics Limited, Cambridge, United Kingdom,
(4) Universite Catholique de Louvain, Louvain-la-Neuve, Belgium,
(5) School of Engineering, University of Warwick, Coventry, CV4 7AL, United Kingdom

12^{45} – 13^{00} **Hall-effect Mobility for a Selection of Natural and Synthetic 2D Semiconductor Crystals**

Scott Monaghan[1], Farzan Gity[1], Jeffrey R. Lindemuth[2], Enrico Napolitani[3], Ray Duffy[1], Gioele Mirabelli[1], Melissa McCarthy[1], Karim Cherkaoui[1], Ian M. Povey[1], Roger E. Nagle[1] and Paul K. Hurley[1]

[1]Tyndall National Institute, University College Cork, Lee Maltings, Cork, IRELAND,
[2]LakeShore Cryotronics, Inc., 575 McCorkle Blvd., Westerville, Ohio 43082-8888, USA.
[3]Dept. Physics & Astronomy, Uni. of Padova & CNR-IMM MATIS, Via Marzolo 8, I-35131 Padova, ITALY

13^{00} – 14^{30} ***Lunch Break***

Session 3: Memory devices

Session Chairs: Francisco Gamiz, Marylin Bawedin

14^{30} – 15^{00} **About the intrinsic resistance variability in HfO_2-based RRAM devices**

C. Cagli[1], G. Piccolboni[1], D. Garbin[1], A. Grossi[1,2], G. Molas[1], E. Vianello[1], C. Zambelli[2], G. Reimbold[1] **(Invited)**

[1]CEA-LETI, Minatec Campus, Grenoble, France,
[2]ENDIF, Univ. of Ferrara, Ferrara, Italy

15^{00} – 15^{15} **ReRAM ON/OFF Resistance Ratio Degradation Due to Line Resistance Combined with Device Variability in 28nm FDSOI technology**

H. Aziza, P. Canet, J. Postel-Pellerin, M. Moreau, J.-M. Portal, M. Bocquet

Aix Marseille Univ., CNRS, IM2NP UMR 7334, 60 rue F. Joliot-Curie, 13453 Marseille Cedex 13, France

15^{15} – 15^{30} **Static Noise Margin Analysis of 8T TFET SRAM Cells Using a 2D Compact Model Adapted to Measurement Data of Fabricated TFET Devices**

F. Horst[1;2], M. Graef[1;2], F. Hosenfeld[1;2], A. Farokhnejad[1;2], G. V. Luong[3], Q. T. Zhao[3], B. Iñíguez[2], A. Kloes[1]

[1]NanoP, TH Mittelhessen University of Applied Sciences, Giessen, Germany, [2]DEEEA, Universitat Rovira i Virgili, Tarragona, Spain, 3PGI 9-IT and JARA-FIT, Forschungszentrum Jülich, Germany

15^{30} – 15^{45} **Design and Implementation Methodology of Energy-Efficient Standard Cell Memory with Optimized Body-Bias Separation in Silicon-on-Thin-BOX**

Yusuke YOSHIDA and Kimiyoshi USAMI

Shibaura Institute of Technology, 3-7-5 Toyosu, Koto-ku, Tokyo, Japan

15^{45} – 16^{00} **Indium-Oxide Nanoparticles for Ox-RRAM in CMOS back-end-off-line**

[1]Edgar A. A. León Pérez, [1]Oumaïma Abouzaid, [1]Khaled Ayadi, [1]Nicolas Baboux, [1]Liviu Militaru, [1]Abdelkader Souifi, [2]Jérémy Moeyaert, [2]Thierry Baron

[1] Institute of Nanotechnologies of Lyon UMR CNRS 5270, INSA de Lyon, 69621 Villeurbanne Cedex, France,
[2] Laboratoire des Technologies de la Microélectronique, Centre National de la Recherche Scientifique, Grenoble, France

16^{30} – 18^{30} ***Poster Session***

20^{00} – ***Reception***

TUESDAY, APRIL 4, 2017

Session 4: Memory devices

Session Chairs: Carlo Cagli, Benjamin Iñíguez

09^{00} – 09^{30} **The mystery of the Z^2-FET 1T-DRAM memory**
Prof. Maryline Bawedin **(Invited)**

IMEP - INP Grenoble MINATEC

09^{30} – 09^{45} **Feasibility Demonstration of New e-NVM Cells Suitable for Integration at 28nm**
S. Kalem[1] and R. Roelofs[2]

[1]BILGEM Informatics and Information Security Research Center, TUBITAK, Gebze, Kocaeli, Turkey , [2]ASM, Kapeldreef 75, Leuven 3001

09^{45} – 10^{00} **Impact of carrier lifetime on Z^2-FET operation**
Mukta Singh Parihar[1], Kyung Hwa Lee[1], Maryline Bawedin[1], Joris Lacord[2], Sébastien Martinie[2], Jean-Charles Barbé[2], Yuan Taur[3] and Sorin Cristoloveanu[1]

[1]Univ. Grenoble Alpes, IMEP-LAHC, Grenoble INP Minatec, CNRS, F-38000 Grenoble, France,

[2]CEA-LETI, Minatec Campus, 38054 Grenoble, France, [3]Univ. of California, San Diego, USA

Session 5: Nanoscale devices

Session Chairs: Sorin Cristoloveanu, Qing-Tai Zhao

10^{00} – 10^{15} **Low temperature performance of proton irradiated strained SOI FinFET**
L.F.V. Caparroz[1], C. C. M. Bordallo[1,2], J. A. Martino[1], E. Simoen[2], C. Claeys[2,3] and P. G. D. Agopian[1,4]

[1]LSI/PSI/USP, University of Sao Paulo, Brazil,
[2]Imec, Leuven, Belgium,
[3]E.E. Dept., KU Leuven, Belgium,
[4]São Paulo State University (UNESP), Campus of São João da Boa Vista, Brazil

10^{15} – 10^{30} **The MSET Transistor as IC Building-Block**
Assaf Peled , Ofer Amrani and Yossi Rosenwaks

t School of Electrical-Engineering, Tel-Aviv University, Tel-Aviv, Israel

10^{30} – 10^{45} **A virtual SOI diode with electrostatic doping**
Kyung Hwa Lee, Maryline Bawedin, Hyungjin Park, Mukta Singh Parihar and Sorin Cristoloveanu

Univ. Grenoble Alpes, IMEP-LAHC, Grenoble INP Minatec, CNRS, F-38000 Grenoble, France

10^{45} – 11^{00} **MOSFETs in the VeSTIC process -fabrication and characterization**
Daniel Tomaszewski, Krzysztof Domański, Grzegorz Głuszko, Andrzej Sierakowski, Dariusz Szmigiel

Division of Silicon Microsystem and Nanostructure Technology, Instytut Technologii Elektronowej (ITE), Al. Lotników 32/46, 02-668 Warsaw, Poland

11^{00} – 11^{30} ***Coffee Break***

Session 6: Nanoscale FETs

Session Chairs: Siegfried Mantl, Manolis Hourdakis

11^{30} – 11^{45} **Silicon tunnel FET with average subthreshold slope of 55mV/dec at low drain currents**

K. Narimani, S. Glass, T. Rieger, P. Bernardy, S. Mantl, Q.T.Zhao

Peter-Grünberg-Institute (PGI9-IT) ,JARA-Fundamentals for Future Technology, Forschungszentrum Jülich, 52428 Jülich, Germany

11^{45} – 12^{00} **Performance and Transport Analysis of Vertically Stacked p-FET SOI Nanowires**

B. C. Paz[a], M. Cassé[b], S. Barraud[b], G. Reimbold[b], M. Vinet[b], O. Faynot[b] and M. A. Pavanello[a]

[a] *Centro Universitário FEI, Av. Humberto de A. C. Branco, 3972, 09850-901 – São Bernardo do Campo – Brazil,*
[b] *CEA-LETI Minatec, 17 Rue des Martyrs, 38054 – Grenoble – France*

12^{00} – 12^{15} **Improved Analog Performance of SOI Nanowire nMOSFETs Self-Cascode through Back-Biasing**

R. Assalti[a], M. Cassé[b], S. Barraud[b], G. Reimbold[b], M. Vinet[b], O. Faynot[b] and M. de Souza[a]

[a] *Department of Electrical Engineering, Centro Universitário FEI, São Bernardo do Campo, Brazil,*
[b] *Département des Composants Silicium – SCME/LCTE, CEA-LETI Minatec, Grenoble, France*

12^{15} – 12^{30} **Dependence of MOSFETs threshold voltage variability on channel dimensions**

C. Couso[1], J. Diaz-Fortuny[1], J. Martin-Martinez[1], M. Porti[1], R. Rodriguez[1], M. Nafria[1], F.V. Fernandez[2], E. Roca[2], R. Castro-Lopez[2], E. Barajas[3], D. Mateo[3], X. Aragones[3]

[1]*Electronic Engineering Department (REDEC) group. Universidad Autónoma de Barcelona (UAB), Barcelona 08193, (Spain),*
[2] *Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, (Spain),*
[3]*Dept. Enginyeria Electrònica, Universitat Politècnica de Catalunya (UPC), Edifici C4, 08034, Barcelona (Spain)*

Session 7: Simulations / characterization

Session Chairs: Cosmin Roman, Panagiotis Sarafis

12^{30} – 12^{45} **Mechanical simulations of BOX creep for strained FDSOI**

R. Berthelon[1,2,3], F. Andrieu[1], B. Mathieu[1], D. Dutartre[2], C. Le Royer[1], M. Vinet[1], A. Claverie[3]

[1] *CEA-LETI, Minatec campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France,*

[2] STMicroelectronics, 850 rue Monnet, B.P. 16, F-38926 Crolles, France,
[3] CEMES-CNRS, 29 rue Jeanne Marvig 31055 Toulouse Cedex 4

12^{45} – 13^{00} **Impact of cryogenic temperature operation on static and low frequency noise behaviours of FD UTBOX nMOSFETs**

B. Nafaa[1,2], B. Cretu[1], N. Ismail[2], O. Touayar[2], E. Simoen[3,4]

[1]Normandie University, UNICAEN, ENSICAEN, CNRS, GREYC, Caen, France,
[2] Carthage University, INSAT, MMA, Tunis, Tunisia,
[3]Imec, Kapeldreef 75, Leuven, Belgium,
[4]Solid-State Physics Department, Ghent University, Krijgslaan 281 S1, Gent, Belgium

13^{00} – 14^{30} ***Lunch Break***

Session 8: Non-Si semiconductor materials and devices

Session Chairs: Max Lemme, Pierpaolo Palestri

14^{30} – 15^{00} **Properties of III-V nanowires**

Prof. Lars-Erik Wernersson **(Invited)**

Lund University, Sweden

15^{00} – 15^{15} **Vertically Stacked Lateral $Si_{80}Ge_{20}$ Nanowires Transistors for 5 nm CMOS Applications**

T. Al-Ameri, A. Asenov

School of Engineering, University of Glasgow, Glasgow, G12 8LT, UK

15^{15} – 15^{30} **Static and LF noise characterization of ultra-thin body InAs MOSFETs**

T.A. Karatsori[1,3], M. Pastorek[2], C.G Theodorou[1], A. Fadjie[2], N. Wichmann[2], L. Desplanque[2], X. Wallart[2], S. Bollaert[2], C.A. Dimitriadis[3], G. Ghibaudo[1]

[1)] IMEP-LAHC, Minatec, BP257, 38016 Grenoble, France,
[2)] IEMN, University of Science and Technology, Lille, France,
[3)] Department of Physics, Aristotle University of Thessaloniki, Greece

15^{30} – 15^{45} **Analysis of the transistor efficiency of Gas Phase Zn Diffusion $In_{0.53}Ga_{0.47}As$ nTFETs at different temperatures**

C. C. M. Bordallo[1,2], J. A. Martino[1], P. G. D. Agopian[1,3], A. Alian[2], Y. Mols[2], R. Rooyackers[2], A. Vandooren[2], A. Verhulst[2], E. Simoen[2], C. Claeys[2,4], N. Collaert[2]

[1]LSI/PSI/USP, University of Sao Paulo, Brazil,
[2]Imec, Leuven, Belgium,
[3]São Paulo State University (UNESP), Campus of São João da Boa Vista, Brazil,
[4]E.E. Dept., KU Leuven, Belgium

15^{45} – 16^{30} ***Coffee Break***

16^{30} – 17^{00} **European Nanoelectronics Research**

Dr Panagiotis Tsarchopoulos, EU Officer

CONFERENCE DINNER

WEDNESDAY, APRIL 5, 2017

Session 9: Novel materials and technologies

Session Chairs: Mireille Mouis, Viktor Sverdlov

09^{30} – 10^{00} **The Prospects of 2D Materials for Ultimately-Scaled CMOS**
Dr. Frank Schwierz ***(Invited)***

University of Ilmenau

10^{00} – 10^{15} **Charge Transport, Interface and Border Traps in Al_2O_3/InGaAs structures**
Y.Y. Gomeniuk[1], Y.V. Gomeniuk[1], A.N. Nazarov[1], S. Monaghan[2], K. Cherkaoui[2], and P.K. Hurley[2]

[1)]V. Lashkaryov Institute of Semiconductor Physics NAS of Ukraine, ISP NASU, Kyiv, Ukraine,
[2)]Tyndall National Institute, University College Cork, Cork, Ireland

10^{15} – 10^{30} **Evaluation of ONO compatibility with high-k metal gate stacks for future embedded flash products**
Adam Dobri[123], Dann Morillon[1], Simon Jeannot[1], Fausto Piazza[1],Carine Jahan[2], Alain Toffoli[2], Luca Perniola[2], Francis Balestra[3]

[1] STMicroelectronics, France ,
[2] CEA-LETI, Grenoble, France , [3] IMEP-LAHC, Université Grenoble Alpes, Grenoble, France

10^{30} – 10^{45} **Hydrogen Silsesquioxane Tri-Dimensional Advanced Patterning Concepts for High Density of Integration in sub-7 nm Nodes**
L. Gaben[1,2,3], S. Barraud[2], V. Balan[2], C. Euvrard[2], S. Pauliac[2], J.-A. Dallery[2,4], J. Bustos[1,2], R. Dechanoz[2], B. Hemard[1,2], L. Koscianski[2], X. Bossy[1,2], C. Arvet[1,2], C. Vizioz[2], S. Barnola[2], C. Perrot[1,2], J. Sturm[2], Y. Exbrayat[2], N. Daventure[2], V. Loup[2], P. Besson[2], B. Perrin[2], B. Previtali[2], M.-P. Samson[1,2], S. Monfray[1], F. Boeuf[1], T. Skotnicki[1], F. Balestra[3], M. Vinet[2]

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[2]CEA-LETI, Minatec campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France,
[3]IMEP-LAHC, Université Grenoble Alpes, BP257, 38016 Grenoble Cedex 1, France,
[4]Vistec Electron Beam GmbH, IlmestraBe 4. 07743 Jena, Germany

10^{45} – 11^{00} **Model 3D MOS capacitor system using regular arrays of vertical Si nanowires**
E. Hourdakis[1], A. Casanova[2], G. Larrieu[2] A.G. Nassiopoulou[1]

[1] NCSR Demokritos, INN, Patriarchou Grigoriou and Neapoleos, Aghia Paraskevi, 153 10 Athens, Greece,
[2] LAAS-CNRS, Université de Toulouse, CNRS, Toulouse, France

11^{00} – 11^{30} ***Coffee Break***

Session 10: Nanoscale MOSFETs

Session Chairs: Jan Hoentschel, Mustafa Badaroglu

11^{30} – 11^{45} **Comparative study of non-linearities in 28 nm node FDSOI and Bulk MOSFETs**

V. Kilchytska[1], B. Kazemi Esfeh[1], C. Gimeno[1], B. Parvais[2], N. Planes[3], M. Haond[3], J.-P. Raskin[1], D. Flandre[1]

[1] CTEAM, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium,
[2] IMEC, Kapeldreef 75, 3001 Leuven, Belgium,
[3] ST-Microelectronics, 850 rue J. Monnet, 38926 Crolles, France

11^{45} – 12^{00} **Sensitivity Analysis of C-V Global Variability for 28 nm FD-SOI**

Krishna Pradeep[1,3], Thierry Poiroux[2], Patrick Scheer[1], Gilles Gouget[1], André Juge[1] and Gérard Ghibaudo[3]

t[1)] STMicroelectronics, Crolles Site, 850 rue Jean Monnet, 38926 Crolles, France,
[2)] CEA-LETI, MINATEC Campus, 38054 Grenoble Cedex 9, France,
[3)] IMEP-LAHC, MINATEC Campus, 3 Parvis Louis Néel, 38016 Grenoble, Cedex 1, France

12^{00} – 12^{15} **Mass data analysis of Random Telegraph Noise in 22nm FDSOI back biased transistors**

Michael Otto, Maximilian Juettner, Jan Hoentschel

GLOBALFOUNDRIES Fab1 LLC & Co. KG, Dresden, Germany

12^{15} – 12^{30} **Strain-induced increase of electron mobility in ultra-thin InGaAs-OI MOS transistors**

Sabina Krivec, Mirko Poljak and Tomislav Suligoj

Department of Electronics, Microelectronics, Computer and Intelligent Systems, Faculty of Electrical Engineering and Computing, University of Zagreb, HR-10000 Zagreb, Croatia

Session 11: Modelling and Characterization

Session Chairs: Enrico Sangiorgi, Asen Asenov

12^{30} – 12^{45} **Compact Modeling of Intrinsic Capacitances in Double-Gate Tunnel-FETs**

A. Farokhnejad[1, 2], F. Horst[1, 2], M. Graef[1,2], C. Liu[3], Q.T. Zhao[3], B. Iñiguez[2], F. Lime[2], A. Kloes[1]

[1]NanoP, TH Mittelhessen University of Applied Sciences, Giessen, Germany,
[2]DEEEA, University Rovira i Virgili, Tarragona, Spain,
[3]PGI 9-IT and JARA-FIT, Forschungszentrum Jülich, Germany

12^{45} – 13^{00} **Assessment of Gate Leakage Mechanism utilizing Multi-Subband Ensemble Monte Carlo**

C. Medina-Bailon[1], T. Sadi[2], C. Sampedro[1], A. Godoy[1], L. Donetti[1], V. Georgiev[2], F. Gamiz[1] and A. Asenov[2]

[1]Nanoelectronics Research Group - CITIC-UGR, Universidad de Granada, 18071 Granada, Spain,
[2]School of Engineering, University of Glasgow, Glasgow G12 8LT, Scotland, UK

13^{00} – 14^{30} ***Lunch Break***

Session 12: Non-Si semiconductor materials and devices

Session Chairs: Anda Mocuta, Heike Riel

14^{30} – 14^{45} **Investigation of InAs/GaSb tunnel diodes on SOI**

[1]C. Convertino, [1]D. Cutaia, [1]H. Schmid, [1,2]N. Bologna, [3]P. Paletti, [4]A.M. Ionescu, [1]H. Riel and [1]K. E. Moselund

[1]IBM Research – Zurich, 8803 Rüschlikon, Switzerland,
[2] EMPA, Electron Microscopy Center, 8600 Dübendorf, Switzerland,
[3]University of Notre Dame, Department of Electrical Engineering IN 46556-5637, USA,
[4]Ecole Polytechnique Federal de Lausanne, EPFL, NanoLab, 1015 Lausanne, Switzerland

14^{45} – 15^{00} **On the electron velocity-field relation in ultra-thin films of III-V compound semiconductors for advanced CMOS technology nodes**

E. Caruso, A. Pin, P. Palestri, L. Selmi

DPIA, University of Udine, Via delle Scienze 206, 33100, Udine, Italy

15^{00} – 15^{15} **GaN-On-Insulator: From QDs to a new substrate**

P. Dimitrakis[1], P. Normand[1], V. Ioannou-Sougleridis[1], C. Bonafos[2] and E. Iliopoulos[3,4]

[1]Institute of Nanoscience and Nanotechnology, National Centre for Scientific Research "Demokritos", P.O. Box 60228, Aghia Paraskevi, 15310 Athens, Greece,
[2]CEMES-CNRS et Université de Toulouse, BP 94347, 31055 Toulouse, France,
[3]Physics Department, University of Crete, P.O. Box 2208, 71003 Heraklion, Greece,
[4]IESL-FORTH, P.O. Box 1527, 71110 Heraklion, Greece

15^{15} – 15^{30} **Modeling the Impact of 2D Hole Gas in a GaN/AlGaN/GaN Heterostructure**

J. Ghosh, S. Ganguly, D. Saha, and A. Laha

Department of Electrical Engineering, Indian Institute of Technology, Mumbai, India

15^{30} : *CLOSING CEREMONY*

POSTER PROGRAM

Poster Session, Monday 3/04/2017, 16^{30} – 18^{30}

P1 **S-shaped Gate-All-Around MOSFETs for High Density Design**

Ya-Chi Huang[1], Meng-Hsueh Chiang[2], and Shui-Jinn Wang[1]

[1]Institute of Microelectronics, National Cheng Kung University, Tainan 701, Taiwan,
[2]Department of Electrical Engineering, National Cheng Kung University, Tainan 701, Taiwan

P2 **C-shape silicon window nano MOSFET for reducing the short channel effects**

Mahsa Mehrad and Elmira Safarpour Ghadi

School of Engineering, Damghan University, Damghan, Iran

P3 **Improving on-state breakdown voltage and double hump substrate current of HV NMOS**

[A, B]Dongil Park, [A]Sungmin Kang, [A]Youngmok Kim, [B]Yonghan Roh and [A]Ohkyum Kwon

[A]LSI TD Team, System LSI division, Samsung Electronics, 1, Samsung-ro, Giheung-gu, Yongin-si, Gyeonggi-do, 17113, Republic of Korea,
[B]College of Information and Communication Engineering, Sungkyunkwan University, 2066, Seobu-ro, Jangan-gu, Suwon-City, Gyeonggi-do, 18448, Republic of Korea

P4 **Effects of Thermal Generation on Reliability of Z^2-FET Device**

[1]Sehyun Kwon, [1]Jinho Ahn, [2]Francisco Gamiz, [3]Sorin Cristoloveanu,[4]Chunkeun Kim, [4]Seong Il Kim, and [4]Yong Tae Kim

[1]Division of Materials Science and Engineering, Hanyang University, Seoul 04763, Korea ,
[2]Nanoelectronics Research Group, University of Granada, 18071 Granada, Spain,
[3]IMEP-LAHC, Grenoble INP MINATEC, 38016 Grenoble, France,
[4]Semiconductor Materials and Device Lab, Korea Institute of Science and Technology, Seoul 02792, Korea

P5 **Effects of non-stoichiometry of silicon oxide layers in double barrier structure on high temperature annealing of ultrathin silicon layer**

Romuald B. Beck[1,2] , Paweł Korb[1]

[1)] Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Warsaw, Poland,
[2)] CEZAMAT PW, Warsaw, Poland

P6 **Experiments and simulation of multilevel resistive switching in forming free Ti/TiO_{2-x} RRAM devices**

P. Bousoulas, I. Giannopoulos, P. Asenov, I. Karageorgiou, and D. Tsoukalas

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P7 **Z^2-FinFET: 1T-DRAM operation**

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P8 **Analog and RF analysis of gate all around silicon nanowire MOSFETs**

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P9 **Experimental comparison between relaxed and strained Ge pFinFETs**

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P10 **Layer Thickness Impact on Second Harmonic Generation Characterization of SOI Wafers**

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P11 **FLEXIBLE PIEZOELECTRIC TRANSDUCERS BASED ON A PMMA/ZNO NANOWIRE COMPOSITE**

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P12 **Analog parameters on pMOS SOI Ω-gate nanowire down to 10 nm width for different back gate bias**

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P13 **Quantum Confined Model for a Novel Tri-Material Gate Stack Engineered Double Gate MOSFET**

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P14 **Characterization of semiconductor structures using scanning microwave microscopy technique**

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P15 **Back Enhanced (BE) SOI MOSFET under non-conventional bias conditions**

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P16 **Improved Electrical Characteristics of Gate-Last FD-SOI TFETs with All ALD High-k/Metal Gate Stack Using D_2 Passivation**

Jae Ho Lee, Donghwan Lim, Andrey Sokolov Sergeevich, Hoon Hee Han, Seok Ki Son, Yu-Rim Jeon, and Changhwan Choi

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P17 **A reliable high performance nano SOI MOSFET by considering Quadruple silicon zones**

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P18 **Is there a kink effect in FDSOI MOSFETs?**

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P19 **Nanoscale electrical characterization of a varistor-like device fabricated with oxydized CVD graphene**

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P20 **Multi-Subband Ensemble Monte Carlo simulations of scaled GAA MOSFETs**

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P21 **FDSOI MOSFET threshold voltage characterization based on AC simulation and measurements**

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P22 **Back-gate bias effect on FDSOI MOSFET RF Figures of Merits and Parasitic Elements**

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P23 **Al_2O_3 coating of nanoparticle networks via ALD: effect on strain-sensing performance**

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P24 **Toward the integration of Si nanonets into FETs**

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P25 **Si measurements: SiO_x on Si**

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P26 **Design and fabrication of a novel power Si/SiC LDMOSFET for high temperature applications**

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P27 **Gate capacitance performance of p-type InSb and GaSb nanowires**

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