S-shaped Gate-All-Around MOSFETs for High Density Design

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***Abstract*—For maximum utilization of layout area using the vertical gate-all-around (VGAA) MOSFETs, this paper proposes a new S-shaped GAA (SGAA) MOSFET structure for 3D integration. The proposed approach improves the layout density per unit cell to extend Moore's Law without the need of aggressive technology scaling. By adjusting the dimensional parameters in the layout schematic, we can tune the device performance such as drive current easily, thus providing a circuit design flexibility for SoC application. Using the same effective channel width for comparison with others vertical GAA structures, the proposed one gives an advantage in better short-channel effects based on three-dimensional TCAD simulation. In addition, by interlacing SGAAs in a repeated unit cell configuration for high density design, just like multi-finger layout, the area density is increased by 3.3x as compared with the ring-shaped GAA MOSFET.**

Keywords- gate-all-around MOSFET; multi-fin; SoC application; vertical structure

I. INTRODUCTION

To maintain historical trends of improved device performance/density, continued scaling of MOSFETs for leading-edge logic technology has driven the industry toward technology innovations including high-k gate dielectrics and strained channels. While minimizing the device size, challenges coming from fundamental physics as a result of scaling require new structures to enable future semiconductor nodes. In terms of electrostatic control to scale to shortest possible channel length, GAA is the ultimate structure. When the gate length scaling is no longer effective due to the limits of contact width, a transition to a vertical structure (Fig. 1 (a)) [1], which is not limited by restriction in the perpendicular direction, is needed. The vertical structure can be implemented in different layout configurations. The gate-all-around ring (GAAR) MOSFET, as shown in Fig. 1 (b) [2], provides a high density solution but has no flexibility in a multi-fin-like layout. Each GAAR is still implemented independently in a given area where the area efficiency is limited to the area percentage of the largest circle within a square. In this paper, we propose an S-shaped GAA (SGAA) MOSFET to improve the area efficiency in vertical structure.

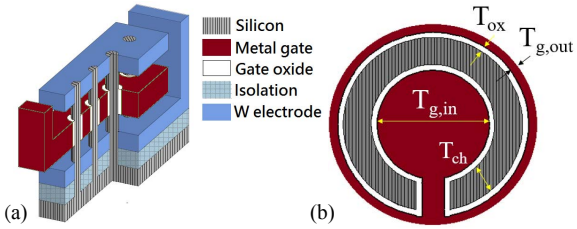

Figure 1. (a) 3-D structure of vertical gate-all-around MOSFET [1] and (b) channel cross section of the GAAR MOSFET [2].

II. S-SHAPED STRUCTURE

Fig. 2 (a) shows our proposed S-shaped vertical GAA MOSFET and Fig. 2 (b) is the cross section at the half channel length. To eliminate the corner effect, the extended turning portion of the channel is rounded. For high density design, the channel gap is fitted by one channel thickness to interlace the SGAA devices one by one. In addition, the outer part of the interlaced structure, i.e. the U-shaped channel which is a half of the S-shaped (1 S-shaped = 2 U-shaped MOSFETs) can be used to achieve high density design, as shown in Fig. 2 (c).

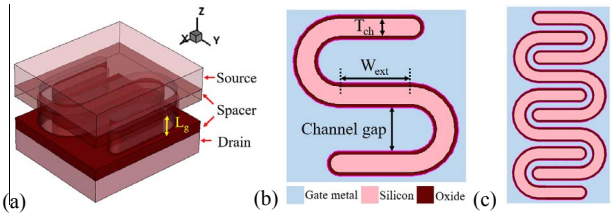

Figure 2. (a) 3-D structure of the S-shaped GAA MOSFET structure, (b) the cross section at the half of the gate length (x-y plane), and (c) interlaced S-shaped structure to improve the density. This is the example for a 3-unit S-shaped structure with an area of 0.00302 μm^2.

In our proposed structure, the design parameters are gate length (L_g), channel thickness (T_{ch}) and extended channel width (W_{ext}) for flexible design. The equivalent oxide thickness was fixed at 1 nm. The gate work function (GWF) was adjusted to meet the off-state leakage current specification. (I_{off} = 100 nA/μm at V_{DS} = 0.68 V) [3] [4]. We simulated the structure using 3-D Sentaurus TCAD with drift-diffusion transport using Philips unified mobility model and high field saturation, Fermi-Dirac statistics, and the density gradient quantization model for quantum mechanics [5].

III. CONCEPTUAL PROCESS FLOW

Based on the same manufacturing technology, the SGAA MOSFET is processed with the same flow for common vertical devices. Fig. 3 shows the conceptual process flow. The silicon substrate is prepared at first, and followed by fin patterning to define S-shaped channel with anisotropic dry etch. Considering the gate fringe capacitances extended to source/drain due to fringe field and impact on parasitic capacitances in the source/drain, it is suggested that the drain region is placed in the bottom of the silicon substrate [6]. The following steps are the spacer deposition at drain, gate metal re-fill, and the spacer deposition at source. The raised source is done in the last step. In contrast to planar structure, the total area now depends on the channel width and channel thickness.

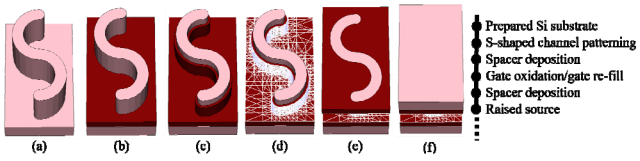

Figure 3. Conceptual process flow of the SGAA MOSFET.

IV. DESIGN OPTIMIZATION AND PERFORMANCE ANALYSIS

Regarding the design optimization of the proposed structure, here we define another standard counterpart with the straight vertical structure for comparison. The current values are normalized to the same effective channel width (e.g. I_{off} = 10^{-7} A/μm). To check the impacts of T_{ch}, W_{ext} and L_g, Figs. 4 and 5 show simulated T_{ch}, L_g, and W_{ext} impacts on on-state current (I_{on}), intrinsic delay time, drain-induced barrier lowering (DIBL), and subthreshold swing (SS), respectively. It is expected that DIBL of the S-shaped channel is better than that of the straight channel due to corner effect. There are the same trends in the L_g and W_{ext} variations. The case of the thinner (T_{ch} small) and longer (L_g large) channel is better due to reduced SCEs. Since the W_{ext} value is proportional to the channel area, it should not extend excessively. However, the performance of longer W_{ext} is better for SGAA with less impact of rounded corner in which the gate control is weaker.

In addition to the performance, we also benchmark the area efficiency for the SGAA MOSFET of L_g = 10 nm, T_{ch} = 5 nm and W_{ext} = 0 nm, and the GAAR MOSFET of L_g = 10 nm, T_{ch} = 5 nm and $T_{g,in}$ = 20 nm. The SGAA and GAAR areas are estimated to be 0.00155 and 0.00152 μm^2 [2], respectively. Their unit cell areas are very close. Note that here we assume that one SGAA is equivalently composed of two GAARs. For high density design, if we repeat the unit cell to construct the multi-fin configuration, the area of GAAR MOSFET is doubled. However, the SGAA MOSFET can be implemented in an interlaced structure, as illustrated in Fig. 2 (c). Fig. 6 (a) shows a 3.3x density improvement of SGAA over GAAR for repeated 10 unit cells. For comparison with VGAA (Table 1), the area density of SGAA is 6x of VGAA (Figure 6 (b)). Increasing W_{ext} (as in Fig. 2 (b)) would improve the density of SGAA even further.

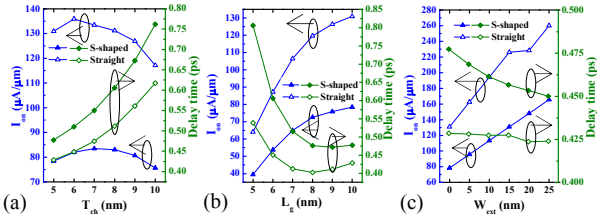

Figure 4. Simulated I_{on} and delay time with (a) T_{ch}, (b) L_g, and (c) W_{ext} variation, respectively.

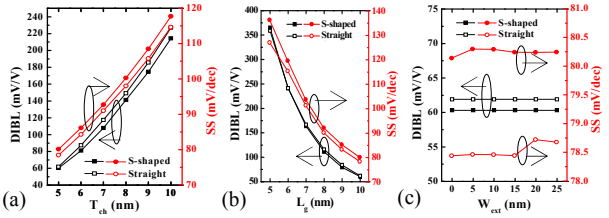

Figure 5. Simulated DIBL and SS with (a) T_{ch}, (b) L_g, and (c) W_{ext} variation, respectively.

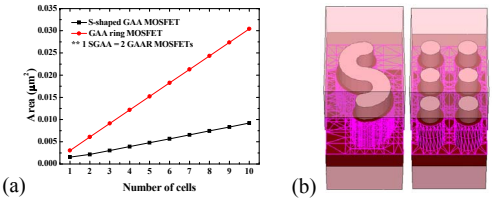

Figure 6. (a) Estimated area comparison of SGAA and GAAR MOSFETs with multi-fin design in terms of unit cell and (b) repeated VGAAs for the same equivalent unit cells of the SGAA MOSFET.

Table 1. Simulated characteristics of a single VGAA cell.

Unit cell	I_{on} (μA/μm)	I_{off} (nA/μm)	DIBL (mV/V)	SS (mV/dec)	V_t (V)	Area (nm^2)
VGAA	599	100	19.05	67.67	0.14	90.25

V. CONCLUSION

This paper has presented the vertical S-shaped GAA MOSFET to improve the area efficiency for high density design. Compared with other vertical structures, SGAA achieves an even higher area efficiency. By simply adjusting the layout parameters, it is flexible to tune the device performance and to achieve the needed density of the vertical structure array.

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C-shape silicon window nano MOSFET for reducing the short channel effects

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***Abstract*— This paper introduces a novel reduced short channel effects nano scale SOI MOSFETs by C-shape silicon window inside the channel, source and buried oxide. This work investigates the main characterizations such as maximum lattice temperature, subthreshold swing, DIBL, threshold voltage roll-off which all of them have better behavior than the conventional SOI MOSFET (C-MOSFET) in case of reliable low-voltage applications. All the achieved numerical results have been extracted by two-dimensional ATLAS simulator.**

Keywords- MOSFET, SOI, Short channel effect, Maximum lattice temperature, Drain current.

I. INTRODUCTION

The development of the electronic industry cannot be considered with neglecting the important role of Metal Oxide Semiconductor Field-effect transistors (MOSFET). Over the past decades, many researchers have tried to increase the quality of this type of transistors [1, 2]. Silicon-on-insulator technology (SOI) is the result of the researchers' efforts for achieving more applicable MOSFET [3, 4]. As the devices are scaled to nanometer regime, the undesirable effects, which are named as short channel effects (SCEs) occur and become more problematic [5, 6]. In order to suppress the short channel effects and decrease the lattice temperature, a new nano SOI MOSFET is presented in this paper. The main idea is using C-shape silicon window that is extended in part of channel, source and buried oxide. However, a part of the buried oxide is removed and is filled by silicon. Applying silicon window with high doping density than channel reduces DIBL, threshold voltage roll-off and subthreshold swing. Also, replacing silicon instead of SiO_2 helps to reduce maximum lattice temperature. The results are extracted from 2D-dimensional ATLAS simulator [7].

II. DEVICE STRUCTURE AND MECHANISM

Fig. 1 shows the schematic of the proposed C-shape silicon window nano MOSFET (CSW-MOSFET). As the figure shows, the C-shape silicon window is extended in the channel, source and buried oxide. This window consists three parts: the top region, middle region and down region. The length and thickness of the top region are defined as $L_{N\text{-}top}$ and $t_{N\text{-}top}$, respectively. It is important to note that the length and thickness of the top region and the down region are the same in the ATLAS simulation. The length and thickness of the middle region have $L_{N\text{-}mid}$ and $t_{N\text{-}mid}$ symbols, respectively. Moreover, the doping density of C-shape silicon window is 1×10^{18} cm^{-3}. The Source/Drain and the channel doping densities are 1×10^{19} cm^{-3} and 1×10^{16} cm^{-3}. The channel length and thickness of silicon on insulator layer are 50 nm and 40 nm, respetively. Top (down) silicon window length and thickness are 50 nm and 15 nm. Middle silicon window length and thickness are 10 nm and 15 nm. Buried oxide thickness (t_{BOX}) and gate oxide thickness (t_{ox}) are 30 nm and 1 nm. Source/Drain length is 30 nm.

III. RESULTS AND DISCUSSION

The important parameter of the nano scale transistors is drain induced barrier lowering (DIBL). Fig. 2 shows the variation of DIBL in different channel lengths. The proposed structure has lower DIBL than conventional MOSFFET (C-MOSFET) because the silicon window reduces the diffusion of the drain electrical field lines to the channel through the buried oxide.

In conventional MOSFET, the holes accumulate in the channel increasing the surface potential. In the proposed structure, the reduced surface potential happens due to the absorbing holes in N^+ window. Fig. 3 shows the subthreshold swing for both structures where better behavior of the proposed structure is clear.

The variation of the threshold voltage in CSW-MOSFET is less than C-MOSFET as it is shown in Fig. 4. So, low dependence of threshold voltage on the channel length in CSW-MOSFET increases the performance of the device.

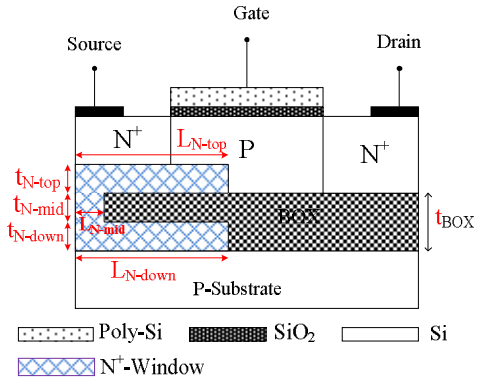

Figure 1. The schematic of CSW-MOSFET.

The leakage current is defined as the drain current when the applied biases are set to the structure. Fig. 5 indicates that the leakage current of the proposed CSW-MOSFET is less than C-MOSFET.

In the proposed structure, the C-shape silicon window is extended to the buried oxide that reduces the maximum lattice temperature as it is shown in Fig. 6 which shows the significant performance of the device in high temperatures.

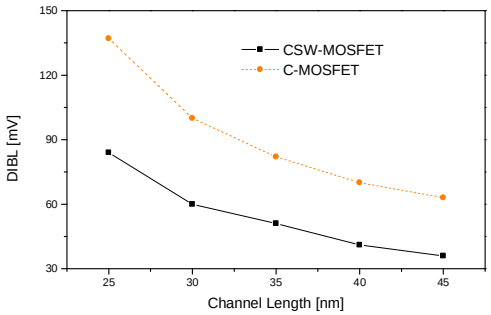

Figure 2. DIBL in different channel lengths for CSW-MOSFET and C-MOSFET.

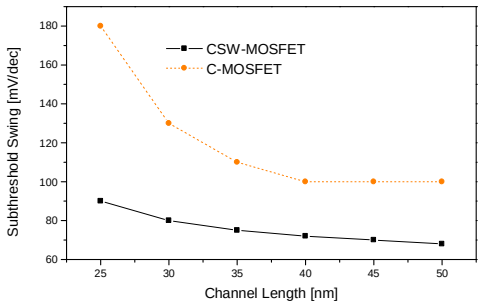

Figure 3. The subthreshold swing for both structures.

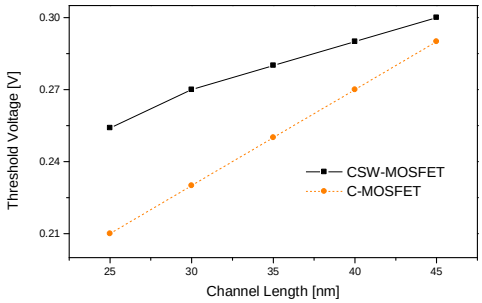

Figure 4. The threshold voltage variation for both structures.

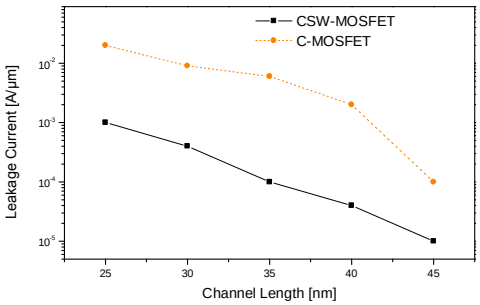

Figure 5. The leakage current for both structures.

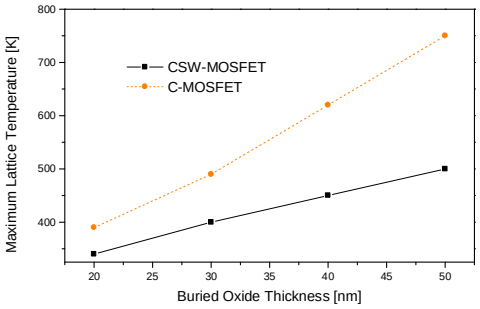

Figure 6. The maximum lattice temperature for both structures

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Improving on-state breakdown voltage and double hump substrate current of HV NMOS

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***Abstract*—We present the on-state breakdown voltage (onBV) characterization of high voltage N-type MOSFET (NMOS). In the low doped drain (LDD) structure, high gate onBV shows worse than low gate onBV because of double hump substrate current (Isub) explained by Kirk effect. Previous researches suggest increasing LDD dopant concentration to reduce the second hump of Isub might cause punch-through leakage worse. We propose the new solution which is the optimization of implantation energy to improve the high gate onBV with suppressing leakage.**

Keywords-High voltage; CMOS; High gate onBV; Double hump substrate current; LDD enginnering;

I. INTRODUCTION

For display driver IC (DDI) applications, 8~18V high voltage MOSFETs are continually integrated to decrease device size while being developed as a high current driver to charge the capacitor of display panels faster for the higher frequency. These technology trends cause that the onBV issue becomes a critical barrier to minimize the device size. Conventionally, the impact ionization peak is shown at the gate voltage under the half of drain voltage. However, according to the Kirk effect [1], impact ionization peak exists at the high gate voltage with double hump Isub in the extended LDD structure [2]. And high gate onBV measured at the maximum gate voltage is lower than low gate onBV measured at the gate voltage of the first Isub peak. This study proposes the optimized implantation to improve the high gate onBV.

II. CHARACTERIZATION AND SIMULATION

Fig. 1 and Fig. 2 show the typical Isub and VDID curve measured at the 18V NMOS. The Isub peak exists at the maximum gate voltage. Fig. 2 shows that high gate onBV caused by snapback occurs at lower voltage than the low gate onBV. And Fig. 3 shows a correlation between Isub peaks and onBV points. To analyze the electric field (e-field), TCAD simulations are conducted. In Fig. 4, the simulation profile based on the standard 0.18um CMOS process is formed by a high voltage P-Well; an extended N type LDD; a shallow trench isolation (STI). Fig. 5 shows the simulated snapback curve at a maximum gate voltage Fig. 6 and Fig. 7 show e-field distributions among the surface of drift region while increasing gate and drain bias. When increasing whichever biases, e-fields move to drain region as well known Kirk effect [3].

III. EXPERIMENTS AND PROCESS OPTIMIZAION

Most qualitatively used way to reduce the Isub double hump is LDD dopant concentration (dose) increasing. Fig. 8 and Fig. 9 plots measured at different dose conditions show significant improvements not only in double hump Isub but also in high gate onBV [4]. However, the punch-through leakage current might be caused by LDD dose increasing is a critical issue to integrate the MOSFETs. The optimization of multi-steps implantation energy can be the advanced solution. Classically, high voltage CMOS have processed long time consuming thermal anneals for a low LDD dose and wide junction profiles. Recently to reduce device size and process time, multi-steps implantation replace the thermal anneal process. The optimized multi-steps doping profile spreading the current density at the edge of the N-type drain suppresses the Kirk effect. Fig. 10 shows measured Isub curves with only different implantation steps' energy. Fig. 11 shows improved High gate onBV. Even a low gate onBV gets worse, it is still higher. Fig. 12 shows the junction profiles of three implantation energy conditions with current density gradations. The spread current density drops the e-field peak and results that high gate onBV increases by 4.2%; e-field peak decreases by 3.0%; low gate onBV decrease by 3.1% as shown Fig. 13.

IV. CONCLUSION

It is discussed that high gate onBV become a critical issue to define the device size in advanced high voltage MOSFET technology for DDI applications. High voltage transistor characterizations are shown by measured data fabricated by 0.18um CMOS process; a simulated data by TCAD. It is demonstrated that the more optimistic way is to optimize the multi-steps implantation energy than LDD dose increasing to suppress leakage current.

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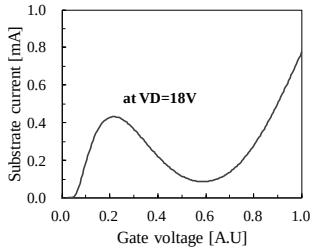

Figure 1. The measured I_B-V_G curve at the 18V high voltage NMOS with extended N-type LDD

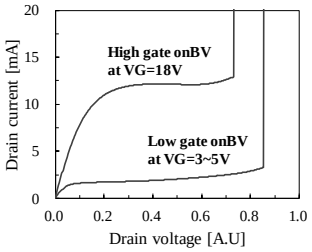

Figure 2. The measured I_D-V_D curve at the 18V high voltage NMOS with extended N-type LDD

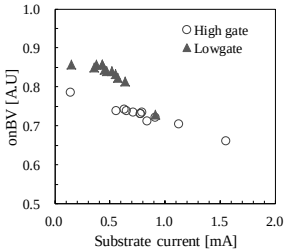

Figure 3. Correlation between substrate current peak(Isub peak) and onBV

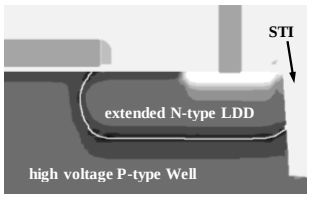

Figure 4. HV NMOS profile from TCAD simulation

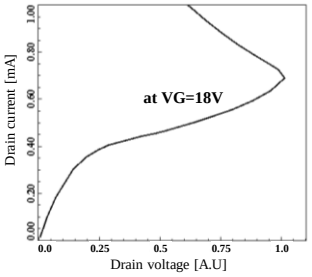

Figure 5. I_D-V_D curve from TCAD simulation

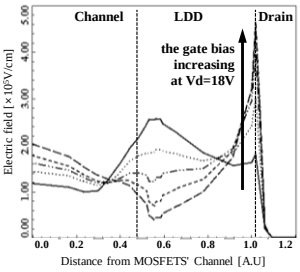

Figure 6. The electric field at the gate bais increasing

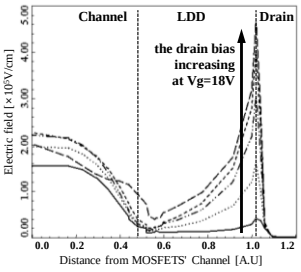

Figure 7. The electric field at the drain bais increasing

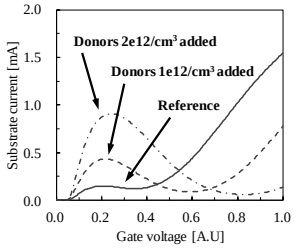

Figure 8. Measured I_B-V_G curve at LDD dose increasing

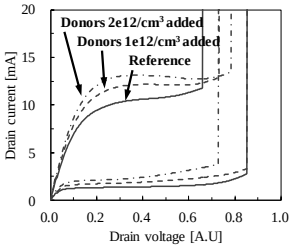

Figure 9. Measured I_D-V_D curve at LDD dose increasing

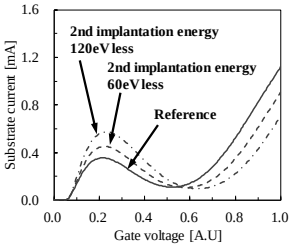

Figure 10. Measured I_B-V_G curve at LDD energy optimization

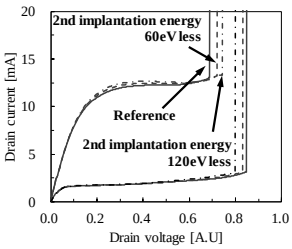

Figure 11. Measured I_D-V_D curve at LDD energy optimization

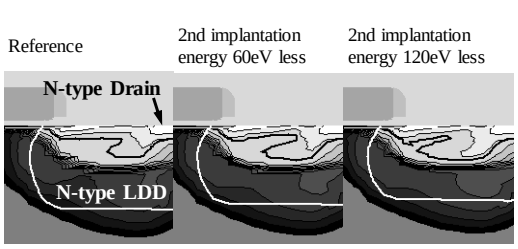

Figure 12. The junction profile of extended N-type LDD with the current density gradation

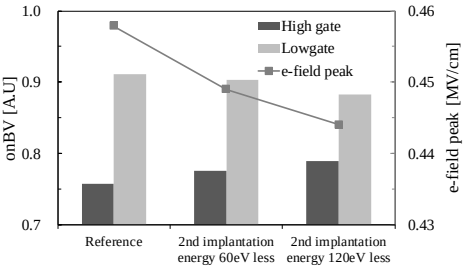

Figure 13. onBVs and e-field peak

Effects of Thermal Generation on Reliability of Z^2-FET Device

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***Abstract*—Electrical characteristics of zero impact ionization and zero subthreshold swing field-effect-transistor transistor (Z^2-FET) has been investigated under the variations of temperature. At 200℃, Z^2-FET shows quite different characteristics; the turn on voltage shifts from -1.2 to -1.5 V after gradual increase of drain current with the increase of drain voltage. The changed characteristics seem to be originated by the thermal generation and we will discuss the effects of thermal generation on reliability in the memory performance of Z^2-FET in detail.**

Keywords-component; Z^2-FET; FD-SOI; Thermal generation, Sharp switch; Hysteresis; Retention time; Memory performance

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I. INTRODUCTION

The thyristor structured single transistor DRAMs (1T-DRAMs), so called Z^2-FET is of great interest due to its great performance in memory device such as very low subthreshold swing, high on/off current ratio, low power consumption and fast access speed [1-4]. However, reliability of Z^2-FET is still not explored in detail [5-7]. For example, we need to investigate the relations between electrical characteristics and temperature since heating in the fully depleted SOI device causes serious problems such as variation of threshold voltage, reduction of mobility, leakage current, and eventually memory array performance. In this study, we have investigated the effects of temperature on electrical characteristics of Z^2-FET. Increasing the temperature from 25 to 200℃, we have studied DC and AC characteristics of Z^2-FET. This research is essential for the reliability of Z^2-FET memory array because shift of switching voltage, swing slope, the drain current before switching on may be sensitive to temperature.

II. EXPERIMENT

In order to investigate the electrical characteristics of the Z^2-FET DRAM under the various operating temperature, we have used Z^2-FET devices provided by INPG. The Z^2-FET device used has a p+ type source with an n+ type drain and an intrinsic channel. The channel is partially covered by the gate on the drain side and a buried oxide layer is below. The length of the channel which is partially covered by the gate (L_G) is 200nm and the length uncovered (L_{IN}) is also 200nm. The width of the device is 10μm. Conventional MOSFET devices operate at moderate temperatures up to 150-200℃. At higher temperatures, these devices usually fail due to increased junction leakage, thermally induced latch-up and threshold voltage shifts [5-6]. So, the high-temperature limit is normally 200℃. Thus, the devices have been tested from 25 to 200℃ to see the effects of temperature. The gate bias V_{Gf} and back gate bias V_{Gb} was fixed at -1.5V and 5V. The drain voltage V_D was swept forward and backward from 0V to -2.5V.

III. RESULTS AND DISCUSSIONS

Figure 1 and 2 show the I_D-V_D curves at 25℃ and 200℃, respectively. At 25℃ the hysteresis curve has about 0.5V memory window and shows sharp switching to '1' state with a very low subthreshold swing. The turn on drain voltage is about -1.2V and on/off current ratio is as high as 10^8. The leakage current at '0' state is very low about 10^{-11}A. This result means that so called the positive feedback [1-4] works very well between electron and hole injection barriers at the source and drain junction. However, when the temperature increases to 200℃, the device shows very different characteristics as shown in Fig. 2. The hysteresis curve seems to be seriously destroyed and the turn on voltage shifts to -1.5V which is increased at the rate of 2mV/℃, and the drain current gradually increases with the drain voltage till the device abruptly switch on. In addition, it does not go to "0" state likely as Fig. 1. At relatively elevated temperature, it is known that a lot of electron and hole pairs are thermally generated [7], and energy barriers at the source and drain junctions are also lowered due to the increased temperature. These carriers form small drain current and slightly increases with drain bias. Meanwhile the electron and hole carriers are injected

into the intrinsic channel due to the lower barriers due to the drain voltage. However, these injected carriers might be recombined with the thermally generated carriers till the injected carriers dominate over the thermally generated carriers. When the injection barriers are lowered enough due to the drain voltage the device sharply turn on due to the positive feedback. Thus, as the temperature increases, the large number of injected carriers are necessary for dominating the thermally generated carriers and the turn on voltage also shifts to higher absolute value to trigger the positive feedback mechanism effectively. From the 1 state to 0 state, these thermally generated carriers are remained and the sharp turn off does not occur. Then, another concerning point related with the thermal generation is that the front gate and buried oxide capacitors may be charged and discharged by the thermally generated carriers at relatively elevated temperature. These charging and discharging may reduce switching speed as shown in Fig. 2, and also influence on the retention time and memory performance. Particularly, heating is more pronounced in fully depleted SOI and the variations of the threshold voltage becomes a function of thinner silicon and buried oxide thickness, and it also causes a reduction of the carrier mobility. We will discuss these issues in detail.

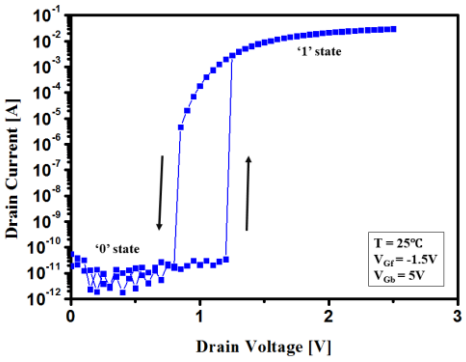

Figure 1. I_D-V_D curve at T=25°C with |V_D|

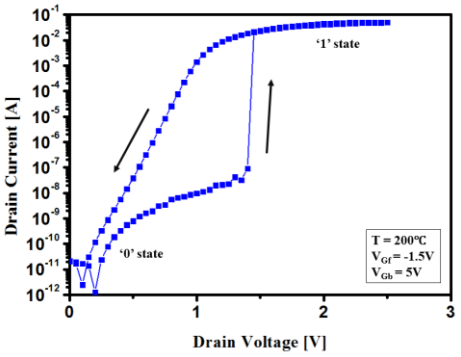

Figure 2. I_D-V_D curve at T=200°C with |VD|

IV. CONCLUSION

High temperature effects on electrical characteristics of Z^2-FET DRAM devices have been studied. The experimental results under the various temperatures from 25 to 200 ℃ show that electrical characteristics are seriously changed at 200℃. These changes seems to be originated by thermal generation. Increasing temperature, the injection barriers at the source and drain junctions will be lowered and the thermally generated electron-hole pairs flow through the lowered barriers, which forms drain current till injected carriers dominate the thermally generated carriers. As a result, fast operations of "1" and "0" states will be occurred with the read/write pulses. Furthermore, these charges may influence on charging and discharging of front and back capacitors, which leads to short retention time and interruption of memory array.

ACKNOWLEDGMENT

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Effects of non-stoichiometry of silicon oxide layers in double barrier structure on high temperature annealing of ultrathin silicon layer

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***Abstract*—Double barrier structure with silicon layer instead of metal can potentially enable variety of intriguing applications of such a structure. The observations so far have pointed out that behavior of such structures during high temperature process may depend on availability of oxygen. It can potentially influence the result of race for silicon atoms between recrystallization and oxidation processes. The aim of this work is to study experimentally influence of excess or deficiency of oxygen (i.e. non-stoichiometric composition) in the barrier oxide layers of this structure (thus having direct contact with ultrathin silicon layer) during high temperature processes in controlled ambient atmosphere.**

Keywords-component; double barrier structure, silicon recrystallization, silicon oxidation, silicon nanocyrstals

I. INTRODUCTION

Double tunneling barrier structures based on metal layer surrounded by ultrathin dielectric layers have been of interest for number of applications, e.g. for memory cells and resonant diodes. Replacing metal with ultrathin semiconductor layer can enlarge the variety of such a structure applications even more.

The main technological stopper for such structures fabrication is, however, a problem of competition between silicon oxidation and its recrystallization during any high temperature process (even with no external oxygen supply). Both of these processes take place simultaneously (e.g. [1]) and thus, final result of high temperature process is potentially dependent and sensitive to free oxygen available in the layers' stack as well as in ambient atmosphere. Another words, any change in composition of oxide barrier layers from stoichiometry can potentially influence kinetics of ultrathin silicon layer oxidation and hence, also - final result of high temperature process.

The aim of this work is to study experimentally influence of excess or deficiency of oxygen (i.e. non-stoichiometric composition) in the barrier oxide layers of this structure.

II. EXPERIMENT

Series of samples were fabricated following the processing sequence shown in the Fig. 1. All deposition processes were performed in Oxford Plasma Technology 80+ PECVD. In order to avoid unnecessary exposure to ambient atmosphere that could provide additional, uncontrolled source of oxygen at the interfaces – the whole sequence was performed simultaneously in the same tool, without venting reactor's chamber.

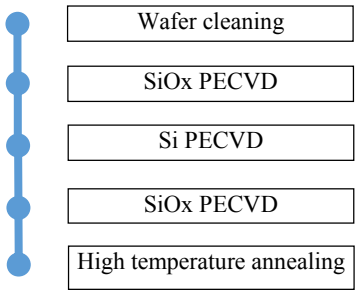

Figure 1. Processing sequence

While conditions of silicon deposition were the same in all cases, PECVD silicon oxide was performed under different conditions in order to achieve either excess of oxygen (x>2), stoichiometry (x≈2) or excess of silicon (x<2) in the obtained SiO_x layers. Difference in silicon-oxygen ratio was achieved by varying ratio of processing gases flows (SiH_4:He/N_2O). Both barrier oxides were fabricated under the same conditions, so that ultrathin PECVD silicon layer once the complete stack was formed was in later stages of processing in contact with the same types of oxides from both sides.

Then, the samples underwent high temperature annealing in pure (6N – 99,9999% purity) argon in high temperature semiconductor type furnace. The annealing conditions were chosen on the basis of previous results [2, 3] (temperatures 800°C and 900°C for annealing times: 1min, 2min and 4 min).

Initial structures, phases and chemical composition, as well as those resulting from high temperature annealing, were studied by means of spectroscopic ellipsometry analysis. Sophisticated, but reliable optical model for this three layers' structure has been developed. The idea of this model is shown in Fig. 2 and has been presented in [4] .

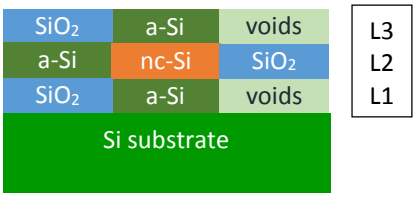

Figure 2. Optical model used for spectroscopic ellipsometry analysis

III. RESULTS

Exemplary results of spectroscopic ellipsometry measurements analysis using presented in Fig. 2 optical model of the double barrier structures fabricated in this study are shown in Figs. 3 and 4. Complete analysis of the received data allowed for drawing number of very interesting conclusions despite the complexity of the studied stacks behavior. They will be presented and discussed in full version of the paper.

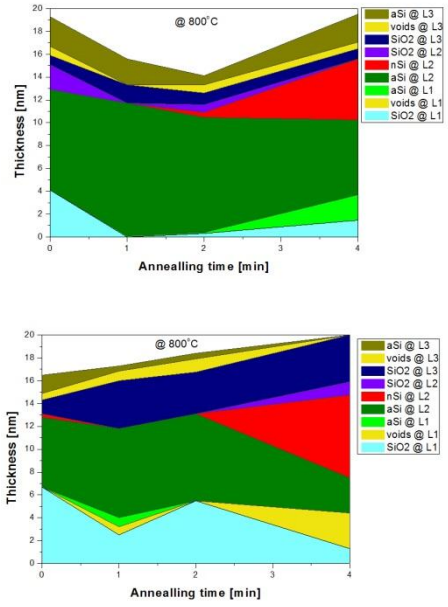

Figure 3. Exemplary results of double barrier structure annealing in 800°C behavior on annealing time and composition of both SiOx layers: a) close to stoichiometry and b) exess of oxygen.

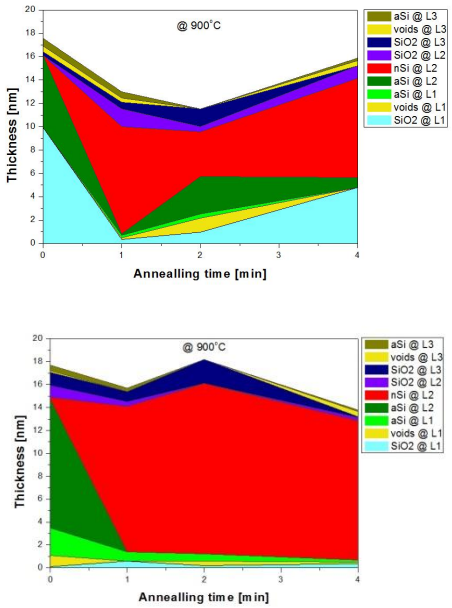

Figure 4. Exemplary results of double barrier structure annealing in 900°C behavior on annealing time and composition of both SiOx layers: a) excess of oxygen and b) exess of silicon.

ACKNOWLEDGMENT

This work was financed partly via National Grants by National Science Centre – DEC-2011/03/B/ST702595 (UMO-2011/03/B/ST7/02595) and by National Centre for Research and Development (NCBiR) under grant No. V4-Jap/3/2016 ("NaMSeN") in the course of "V4-Japan Advanced Materials Joint Call".

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Experiments and simulation of multilevel resistive switching in forming free Ti/TiO_{2-x} RRAM devices

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***Abstract*—Although multilevel capability is probably the most important property of resistive random access memory (RRAM), it is vulnerable to reliability issues due to the stochastic nature of conducting filaments (CFs) creation. As a result, the various resistance states cannot be clearly distinguished which leads to memory capacity failure. In this work due to the gradual resistance switching pattern of TiO_{2-x} RRAM devices, we demonstrate six resistance states with promising temporal variability. It is shown that the formation of small CFs with high density of oxygen vacancies enhances the uniformity of the switching characteristics in spite of the random nature of switching effect. The simulation process is conducted by considering the total bi-layered structure in a 3-D geometry, as well as the configuration of the electrode materials and their impact on the CFs properties.**

***Index Terms*— sputtering, thin films, resistive memory devices, oxygen vacancies, trap-assisted tunneling.**

I. Introduction

THE incessant desire for device scaling has pushed both academia and industry into alternative concepts in order to meet the future information storage needs. Among the potential non-volatile memory candidates, RRAM based on metal oxides seem to gain significant ground in the non-volatile memory race, mainly due to their simple structure and high integration density [1]. At the same time, there is a growing body of evidence that formation/annihilation of CFs are responsible for the reversible switching effect [2]. One of the most important features in memory technology is increased storage density which could enable the fabrication of multibit memory arrays. Since multilevel capability can substantially increase the storage capacity, it is essential to explore new methods in order to enhance this property. Multilevel switching has been reported in many oxide materials and device configurations [3] and although it can be easily attained, careful control over the various resistance states should be ensured, in order to sustain a clear memory window especially under consecutive cycling operation. The reason for these fluctuations is the inherent random nature of CFs formation and the variation of the total number of oxygen vacancies within the CF.

In this study we report high multilevel resistance switching of room temperature deposited TiO_{2-x} thin films with enhanced uniformity properties, which are attributed to the high density of oxygen vacancies inside the CFs. Conical CFs with different diameters were assumed, in order to account for the increased multilevel capability of our devices.

II. Device Fabrication and Electrical Characterization

A. Experimental

The configuration of the memory device used was the following: Au/Ti/TiO_{2-x}/Au, while the fabrication details are reported in our previous work [4]. The sample with the low oxygen content (20%) was used for this work. The oxide film had a thickness of 45 nm. The electrical characterization was carried out with an HP4140B picoamperometer, while ns pulses were applied with an HP8116A pulse generator. During all electrical measurements the bottom electrode (BE) was grounded and the external inputs were applied to the top electrode (TE).

B. DC Device Characteristics and Discussion

Multilevel and forming-free resistive switching performance was achieved by varying the I_{cc} from 5 μA to 5 mA while recording hysteresis loops between -5 V and 5 V (Fig. 1). We remark that in the inset we show the area dependence curve of the measured current. The smallest area devices were of crossbar architecture using gold electrodes of 50 nm width size fabricated by e-beam lithography.

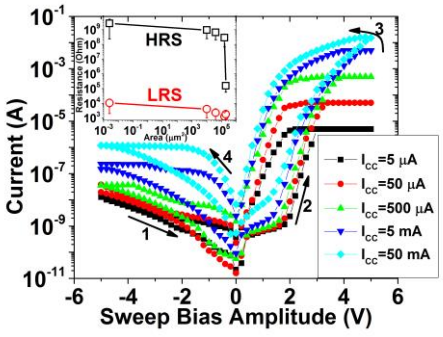

Fig. 1. (a) Measured I-V (sweep rate 1 V/s). The arrows in the graphs signify the switching direction, while the inset depicts the area dependence of both resistance states.

C. Device Numerical Modelling

In order to get a better insight into the origins of the enhanced multilevel switching capability of our devices, we quantitatively investigate the origins of the resistive switching effect. The transport of oxygen vacancies can be predicted by the drift-diffusion, carrier continuity and Joule heating equations, which were solved consistently with a numerical solver (COMSOL) [5, 6]:

$$\frac{\partial n_D}{\partial t} = \nabla \cdot (D \nabla n_D - v \cdot n_D) + G \quad (1)$$

$$\nabla \cdot \sigma \nabla \psi = 0 \quad (2)$$

$$-\nabla \cdot k_{th} \nabla T = J \cdot E \quad (3)$$

where n_D is the concentration of oxygen vacancies, $D = \frac{1}{2} \cdot a^2 \cdot \nu_0 \cdot \exp(-\frac{E_a}{k_B T})$ is the diffusivity, a is the effective hopping distance (0.05 nm), ν_0 is the attempt-to-escape frequency (10^{13} Hz), k_B is the Boltzmann constant, T is the temperature, ψ is the electric potential, E is the electric field, Q is the ion charge (2q), E_a is the diffusion barrier for ionic migration (1 eV), and $v = a \cdot \nu_0 \cdot \exp(-\frac{E_a}{k_B T}) \cdot \sinh(\frac{QEa}{k_B T})$ is the drift velocity. A detailed description of the used models can be found in ref. [5], [6], while both active oxide and electrodes were considered during the simulations.

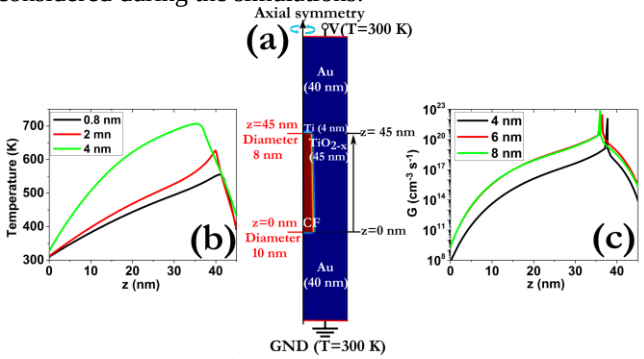

Fig. 4. (a) Cross-section of the simulated cell. A uniform density $n_D = 1 \times 10^{22}$ cm^{-3} was selected for the CF region, Calculated 1D line profiles of (b) T and (c) G for three different CF diameters for RESET (-2 V) and SET (+5 V) transitions, respectively.

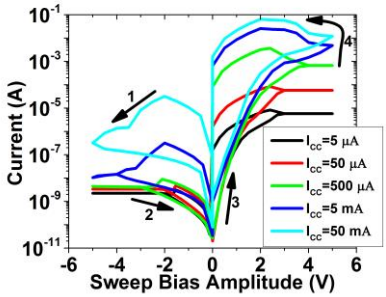

Fig. 5. Calculated I-V characteristics, while the arrows indicate the switching direction.

A depiction of the simulated cell is presented at Fig. 4(a), while in Fig. 4(b) and (c) the local temperature and generation rate profiles for the RESET/SET processes respectively, are displayed. The region where the gap will form strongly depends from the thermal conductivity of the TE, while the BE has a minor effect due to the presence of a thick TiO_x layer. Materials with large thermal conductivity will give rise to the formation of the depleted gap far from the oxide/TE interface, due to the confinement of the produced Joule heating (Fig. 6).

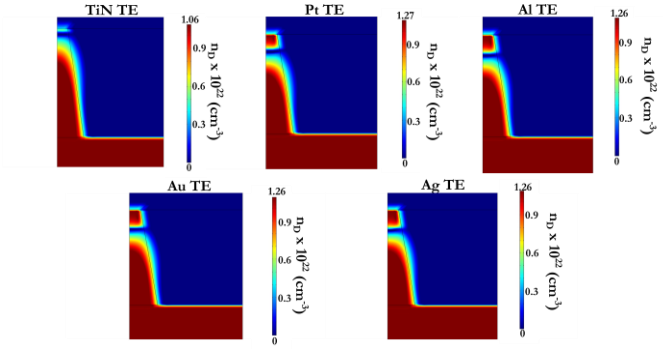

Fig. 6. Calculated map of oxygen vacancy density (n_D) in bilayer TiO_{2-x}/TiO_{2-y} configurations for different protective layers, with same thickness (40 nm) while Ti layer was maintained for all employed electrodes.

III. CONCLUSION

In summary, enhanced multilevel resistive switching performance were demonstrated with low variability in TiO_{2-x}, sputter deposited thin films which is attributed to the small size of CFs with high density of oxygen vacancies. The later has also a pronounced effect during SET transition, imposing a gradual switching pattern, Opportunities for low power and high uniform multilevel capabilities arise also by creating even smaller CFs with high density of oxygen vacancies.

ACKNOWLEDGMENT

Two of the authors (P. Bousoulas and D. Tsoukalas) would like to acknowledge financial support from Research Projects for Excellence IKY (State Scholarship Foundation)/SIEMENS.

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Z^2-FinFET: 1T-DRAM operation

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***Abstract* - In this work, a Z^2-FinFET device structure is suggested and its DC characteristics (I_D-V_D) and 1T-DRAM transient operation are investigated by using the Silvaco ATLAS3D tool. The DC of the Z^2-FinFET shows a very sharp switching, with high I_{On}/I_{Off} ratio (>10^4), around a V_D value, V_{On}. This On voltage can be modulated by adjusting the biases applied to gate and substrate. The operation of the Z^2-FinFET device as capacitor-less memory cell is also shown.**

I. Introduction

The Z^2-FET is a forward biased, partially gated, P-I-N diode with an undoped ultrathin silicon film on a SOI substrate. For a N-type Z^2-FET, the cathode (N^+ doped source) is grounded and the anode (P^+ doped drain) is positively biased. The front-gate (V_{FG}) and back-gate (ground-plane, V_{BG}) are biased to form a virtual NPNP structure. Several papers [1, 2] have been reported about the concept, operation and characteristics of the planar Z^2-FET, but the implementation in 3D architectures has not been addressed, Fig. 1. The forward I_D-V_D characteristics of the 3D device show a very sharp switch at a drain voltage (V_{On}) that depends on the biasing of other terminals, Fig. 2. A very large I_{on}/I_{off} ratio (>10^4) is observed. The backward scan of the drain voltage, might also show a sharp switch from I_{on} to I_{off}, but at different (lower) V_D voltage (V_{Off}, not shown). This behavior suggests a functional Z^2-FET device that could be also operated as 1T-DRAM memory cell using the same 28 nm FDSOI technology. The present work aims to explore if a SOI FinFET structure could be used as seed for a Z^2-FinFET maintaining the sharp switching and DRAM operation. SOI FinFETs are known to feature easy fabrication, excellent electrostatic control and scalability (no shallow trench isolation (STI) required [3]), and they have no leakage path near the source/drain junction regions. Due to resemblance, Z^2-FinFETs would also yield similar characteristics.

II. Simulation Conditions

The DC characteristics and the memory operation of a Z^2-FinFET are investigated by using Silvaco Atlas3D. The Z^2-FinFET structure mimics the planar design but the front-gate surrounds the whole Si-channel as sketched in Fig.1a.

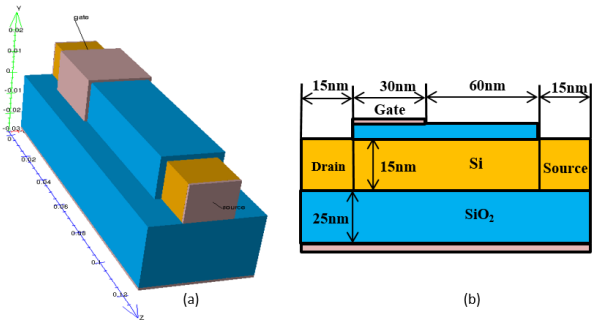

Figure 1. (a) 3D view of the simulated Z^2-FinFET and (b) the lateral cross section from drain to source.

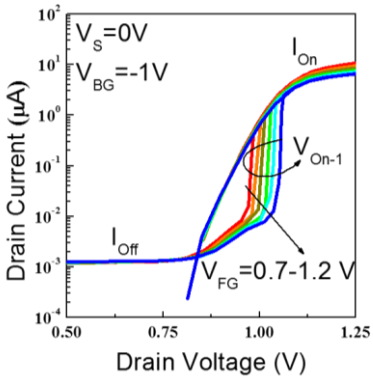

Figure 2. Simulated DC I_D-V_D characteristics for the Z^2-FinFET. Similar structure to Fig. 1.

Fig. 1b presents a lateral (drain to source) cross-section of the simulated architecture. The metal gate length is 30 nm and lies above a 2 nm SiO_2 front oxide. The 15 nm long source/drain feature a doping concentration of $N_{S/D}$=10^{20} cm^{-3} while the channel is N_A=10^{14} cm^{-3}. The gated/ungated length is 30/60 nm leading to a final 90 nm active region length. The thickness/width of Si channel and BOX is 15 nm and 25 nm, respectively. The bipolar model was employed to account for both electron and holes continuity equations. Selberher impact ionization and standard band-to-band tunneling were also included although their impact turned out to be limited. No quantum effect correction was introduced given the thick Si-film.

III. RESULTS AND DISCUSSIONS

Fig. 2 shows the simulated DC characteristics (I_D-V_D) of the 3D Z^2-FinFET. The back-gate and source terminals are fixed to -1V and 0V, respectively. The front-gate voltage is changed from 0.7 V to 1.2 V. The hysteresis curves show the steep transition in the drain current with a rising of the On voltage when increasing the front-gate bias. Fig. 3 exhibits the transient behavior of this device. The drain (dashed) and front-gate (solid) bias patterns are illustrated in Fig. 3a and correspond to a W0-R-W1-R sequence with holding (H) operations in-between. Detailed information regarding the writing (W1), erasing (W0) and reading (R) bias patterns can be found in [1]. The readout drain current is shown in linear and log scale in b). Notice that Fig. 3 demonstrates how the 3D Z^2-FinFET successfully operates as a 1T-DRAM memory cell. The erasing (W0) operation leads to a low-conductivity state while the writing (W1) yields much higher current densities. In stationary conditions (or after W1), the high mobile carrier population in the body screens the vertical electric field induced by the front and back gates and the energy barriers height are reduced.

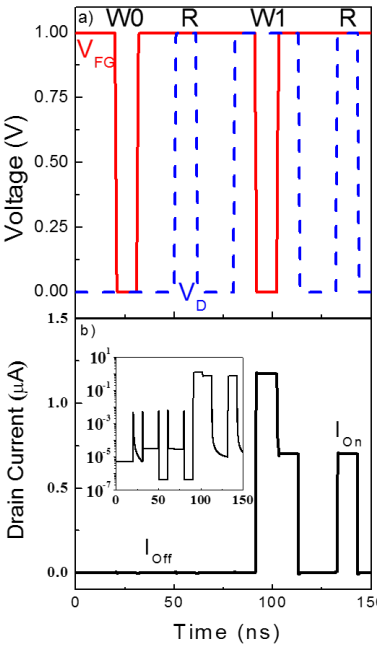

Figure 3. Simulated transient characteristics for a Z^2-FinFET. a) V_{FG} (solid) and V_D (dashed) bias pattern and b) current readout. Inset is the current in log scale. Similar structure to Fig. 1. Rising/falling times are set to 1 ns.

The chosen drain voltage while reading (R), $V_{D\text{-}R}$, must be larger than the DC ('1'-state) On voltage,$V_{On\text{-}1}$ (Fig. 3) for the selected V_{FG} (+1 V). This implies that the readout current after a W1 is high, I_{On}. After a W0, the evacuation of carriers, especially under the gated part of the channel, produces a temporary increase of the energy barriers height (as for the deep-depletion regime in a MOS capacitor [4]), thus a temporary increase of the On voltage is obtained (satisfying $V_{On\text{-}0} > V_{On\text{-}1}$). This is similar to an increase of V_{FG}, Fig. 2. Therefore, if the drain is pulsed to the same $V_{D\text{-}R}$, now $V_{D\text{-}R} < V_{On\text{-}0}$, and I_{off} is obtained. Huge current ratios are extracted, over 10^4 A/A with no dedicated optimization.

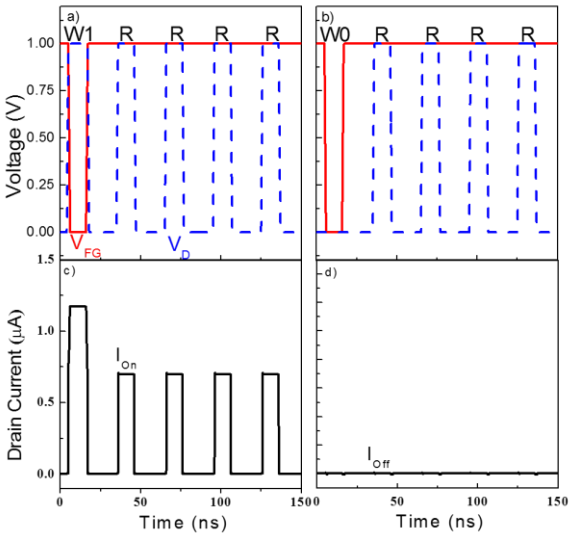

Figure 4. The operational sequence of the Z^2-FinFET for a-c) '1' and b-d) '0' array states. a-b) V_{FG} (solid) and V_D (dashed) bias pattern and c-d) current readout.

Fig. 4a-c (respectively b-d) shows a sequence of multiple consecutive readings of a '1' ('0') state. After a writing W1 (W0) pulse, an array of 5 consecutive reading pulses are applied. No error is observed.

We have demonstrated that Z^2-FinFET device shows a similar behavior to its planar FDSOI counterpart. Simulated DC I_D-V_D characteristics show a very sharp switching at a given V_{ON} voltage which depends on the gates biases. In addition, the device has been sucessfully operated as a 1T-DRAM memory cell. Therefore, Z^2-FinFET joins the advantages of FinFETs and planar Z^2-FETs.

ACKNOWLEDGMENT

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Analog and RF analysis of gate all around silicon nanowire MOSFETs

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***Abstract*— Gate all around (GAA) nanowire MOSFETs with gate length of 130 nm were fabricated on SOI wafers. The analog performance was analyzed in terms of transconductance, output conductance, voltage gain, Early voltage and transconductance efficiency. The RF characterization showed relatively low cutoff frequency and maximum oscillation frequency. Small-signal parameters are extracted using cold FET method combining with an optimization procedure called Artificial Bee Colony (ABC) method. It proves that large parasitic capacitance and high RF output conductance are the main reasons for the degraded RF performance.**

Keywords- Analog; RF; MOSFET; silicon nanowire; SOI;

I. INTRODUCTION

RF performance of silicon MOSFETs has been improved by the aggressive CMOS scaling. Especially the introduction of SOI technology offers great advantages of higher operating speed, more efficient power consumption and lower noise. FinFETs have already shown excellent gate control over SCE (short channel effect). However, nanowire MOSFETs with GAA configuration provide even better electrostatics, aiming for extremely small devices beyond 10 nm node. RF performance of FinFET is degraded because of high parasitic capacitance compared with their planar counterpart. In this work, we investigate the analog and RF performance of GAA nanowire MOSFET.

II. EXPERIMENT

The devices were fabricated in the Helmholtz Nano Facility (HNF) Juelich. SOI wafers with 145 nm BOX (buried oxides) and 40 nm top silicon were used. Nanowires with a width of 25 nm and a gate length of 130 nm are defined with electron beam lithography (EBL). Fig. 1 shows the SEM images for the device structure. GSG (Ground-Source-Ground) structures were also fabricated for RF measurement. S-parameters were measured with 0-40 GHz VNA (vector network analyzer).

III. DISCUSSION

A. Analog Characterization

The transfer and output characteristics of the GAA MOSFET measured at low V_d (0.2 V) are shown in Fig. 2. The device showed a high I_{ON}/I_{OFF} ratio of 10^9 and a subthreshold swing SS of 90 mV/dec. As the nanowires are already very narrow, the relatively large SS is attributed to high D_{it} at the HfO_2/Si interface because of the nanowire roughness and non-optimized ALD process. All analog parameters are extracted under saturation regime (V_d = 1.1 V). The transconductance G_m in Fig. 3(a) shows peak value of 450 mS/mm. Fig. 3(b) shows the voltage gain calculated from the transconductance G_m and output transconductance G_d. The output conductance increases rapidly at large drain current level. Maximum voltage gain appears at a position close to G_m peak, which corresponds to weak inversion. The peak voltage gain is 40 dB. The Early voltage in Fig 3(c) also shows large value of 18 V. G_m/I_{ds} characterizes the efficiency of converting drain current to transconductance. Its peak value is 25 V^{-1} (Fig. 2(d)). All these values are comparable to FinFETs [1].

B. RF Characterization

The current gain cutoff frequency (f_t) and the maximum oscillation frequency (f_{max}) (Fig. 4(a)) are extracted and they are, respectively, 14.8 GHz and 1.75 GHz, which are lower than state-of-art devices. To reveal the reasons for the low cutoff frequency, we make use of a NQS (non-quasi-static) small-signal model to extract small-signal lumped elements. The model is shown in Fig. 4(b) [2]. Cold FET method was used to analytically extract the parameters [3]. However, most extracted parameters vary with frequency. To get reasonable parameters, artificial bee colony (ABC) optimization procedure was used to find out the only solution [4]. During the optimization procedure, trial solutions were selected around the above mentioned analytical solution. The measured S-parameters and fit S-parameters are drawn on polar coordinates (Fig. 5). The most important parameters are listed in Table 1. The intrinsic gate

capacitance C_{gsi} amounts to only 21 fF. However, the parasitic capacitances C_{gse} and C_{gde} dominate the total gate capacitance with value of a few hundred fF. We noticed that the cutoff frequency was also limited by the large output conductance, with $g_d/g_m = 4.5$. This large g_d might be caused by substrate coupling and self-heating effects [5]. The BOX was quite thin after partially removing SiO_2 below the silicon nanowires, thus source drain coupling through substrate enhanced. Self-heating effect is prominent in nanowire devices, but its dynamic component is suppressed at RF frequencies, which can also increase g_d [5].

IV. Conclusion

GAA silicon nanowire MOSFETs are suitable for analog applications. Due to the large parasitic capacitance and output conductance, the cutoff frequency is limited. Optimization of the device structure is necessary to increase the RF performance. In principle, these limitations can be overcome by shrinking nanowire pitch size and using high resistivity SOI substrates.

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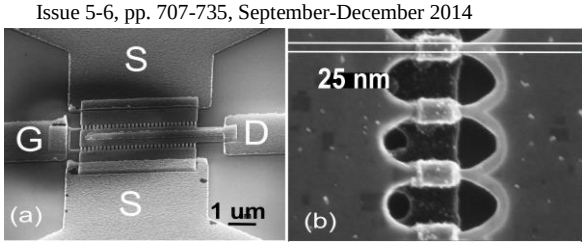

Figure 1. (a) Side view of finished device with Source, Drain, and Gate labeled. (b) Top view of gate on nanowires

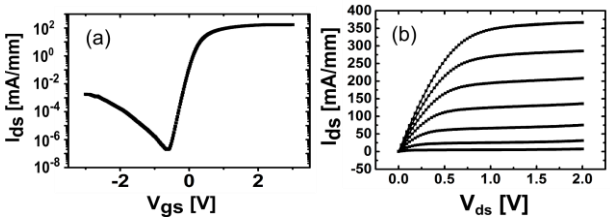

Figure 2. (a) Transfer curve at $V_d = 0.2$ V. (b) Output curves.

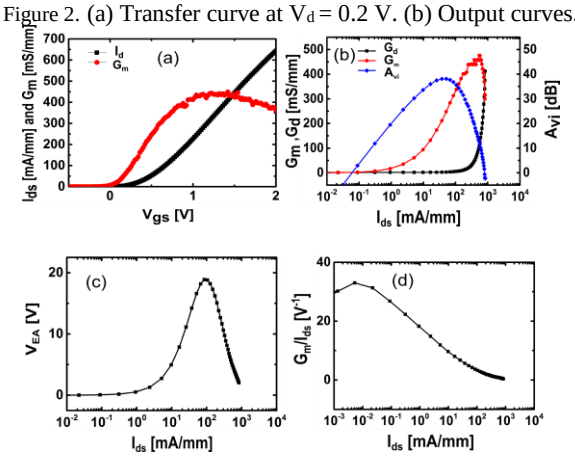

Figure 3. (a) Transconductance and drain current. (b)Transconductance(red), output conductance (black) and voltage gain(blue). (c) Early voltage. (d) Transconductance effeciency.

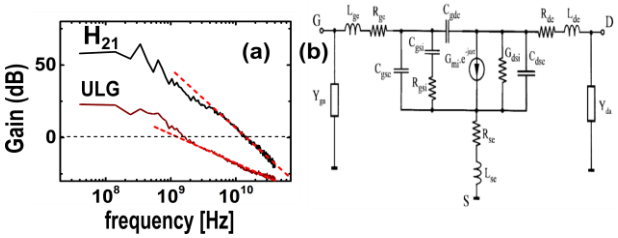

Figure 4. (a) H_{21} and ULG vs frequency. (b) small-signal model.

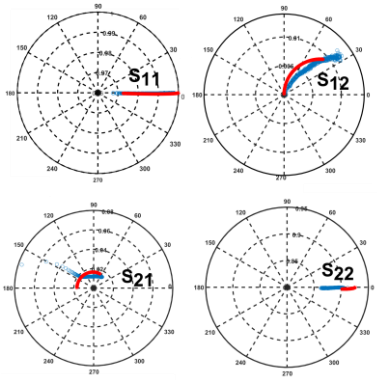

Figure 5. Measured S parameters (blue) and fit (red) on polar coordinates.

TABLE 1. Extracted RF parameters

g_m (mS)	g_d (mS)	C_{gsi} (fF)	C_{gse} (fF)	C_{gde} (fF)
20.4	90.1	21.2	561.8	140.7

Experimental comparison between relaxed and strained Ge pFinFETs

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***Abstract*—The experimental comparison between relaxed and strained Ge pFinFETs operating at room temperature is discussed. Although, the strain into the channel improves the drain current for wide transistors due to the boost of hole mobility, the gate stack engineering has to be further studied in order to solve the threshold voltage shift. The relaxed channel achieves a lower subthreshold swing compared to the strained one, since the latter presents a higher source/drain leakage current. Considering a figure of merit for analog applications, i.e., intrinsic voltage gain A_V, no relevant difference between the relaxed and strained channel performances has been shown for short devices while the relaxed ones present a higher Av for longer devices.**

Keywords-FinFET; germanium; p-type; strained; relaxed

I. INTRODUCTION

The germanium FinFET has been under the spotlight since the combination of high mobility materials and multiple gate devices turned out to be a promising alternative for future high performance applications [1-3]. However, an important challenge is the Si-platform integration, which gives rise to extensive defect generation, mainly misfit (MD) and threading dislocations (TD) [4], due to a mismatch in lattice parameter between Si and Ge [5]. The TD density must be as low as possible, since it degrades the device performance [6, 7]. Therefore, different approaches have been developed in order to grow high-quality Ge on a silicon substrate [8]-[10].

This paper aims to compare the performance of relaxed and strained Ge pFinFETs fabricated in a Shallow-Trench-Isolation (STI) last process. The latter are based on silicon platform integration, taking into consideration not only the impact on the current-voltage (I-V) curve, transconductance (gm), threshold voltage (V_T) and subthreshold swing (SS), but also on output conductance (g_D) and intrinsic voltage gain (A_V). The studied channel length range is from 200 nm to 1000 nm for two fin widths; 20 nm (narrow device) and 100 nm (planar-like device).

II. EXPERIMENTAL DETAILS

The devices used in this work have been fabricated on a p-type silicon substrate at imec/Belgium. Figure 1 schematically shows the two different STI last processes under evaluation in this work, strained and relaxed channels. The compressive biaxial strained channel has a predefined fin in a thin Ge layer (~ 30 nm). The latter has been grown on top of a thicker (1 µm) $Si_{0.3}Ge_{0.7}$ strain-relaxed buffer (SRB) layer on a silicon wafer. The relaxed one is defined in a thicker Ge layer, which has been grown directly in the Si substrate. All data were measured at room temperature. TABLE I. presents the main characteristics and dimensions for both strained and relaxed channels.

III. RESULTS AND DISCUSSION

Figure 2 presents the drain and substrate currents for strained and relaxed pFinFETs for different fin widths (W_{fin}). One clearly observes the impact of the strain effect on the drain current for the planar like device (W_{fin} = 100 nm) in strong inversion regime, where the hole mobility is dominant and enhanced by the compressive strain into the channel. On the other hand, i.e., narrow fin, the same behavior is not found, which indicates either no effective strain impact or the presence of a source/drain leakage current under the fin (due to an over recess of the fin). Apart from that, the substrate current (I_B) noticeably dominates the off current (I_{OFF}). The latter is W_{fin}-independent for both processes. Moreover, the relaxed devices present the highest I_B level, as a result of a higher reverse current of the pn-junction from the drain/substrate [7], due to a lower bandgap of the substrate [11]. In addition, the relaxed devices present a higher Threading Dislocation Density (TDD) level compared to the strained ones [9, 12], resulting in an increase of the substrate current [7].

Figure 3 reveals that wide strained devices present higher transconductance (gm) values than the relaxed ones for all channel lengths, even with a lower gate capacitance density (C_{OX}) due to an inferior Equivalent Oxide Thickness (EOT). Therefore, the strain into the channel boosts the hole mobility. On the other hand, narrow relaxed channels show superior gm performance rather than the strained ones, possibly associated to high C_{OX} value, strain relaxation into the strained device and the presence of source/drain leakage current under the fin (due to an over recess of the fin).

The latter is reinforced from Figure 4, since it points out that strained FinFETs present higher SS values than the relaxed ones, thus, the presence of source/drain leakage current adding to possibly a higher interface state density plays a role in the strained devices. As a result, there is a degradation of the drain current and transconductance for the narrow strained FinFET, as shown in Figure 2 and Figure 3, respectively. In addition, Figure 4 also depicts a constant subthreshold swing (SS) value for both strained and relaxed devices as a function of channel length. The SS parameter shows a W_{fin}-independence for the relaxed devices in the channel length range under consideration.

Figure 5 shows the threshold voltage (V_T) for both strained and relaxed devices, where one clearly notices the difference between V_T values of both channels, ranging from 0.3 V to 0.4 V, as a consequence of compressive strain into the channel that decreases the bandgap [13] and, therefore, the threshold voltage.

The transconductance in saturation operation is presented in Figure 6 and shows the same behavior found as in Figure 3 (linear operation), where narrow and wide devices have similar performance for relaxed channel due to the sidewall contribution to the hole mobility. For the strained devices, the

strain effect on the carrier mobility is evident only for the wide device, since the narrow one might be dominated by a leakage current, therefore, the gm value is equal for the studied channel length range.

Figure 7 reveals that strain engineering into the channel does not play an important role in the output conductance (g_D), at least for short devices. This suggests that the penetration of the lateral electric field has a similar behavior in both relaxed and strained devices, except for long devices where the relaxed one presents better results, i.e, lower g_D value.

Despite that the intrinsic voltage gain (A_V) (Figure 8) presents slightly lower values for the strained channel compared to the relaxed one, its A_V value seems to be more or less constant for short channel lengths, while long relaxed channel devices show a superior performance.

IV. Conclusions

The strained channel is a good alternative for boosting the device performance in digital applications, although, there is a threshold voltage shift, which requires an effort in the gate stack engineering to overcome this issue. On the other hand, from an analog application viewpoint, i.e., focusing on the intrinsic voltage gain, strain into the channel plays no significant role for short devices as the relaxed and strained channels show similar performance.

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TABLE I. Main dimensions and characteristics

	Strained channel	Relaxed channel
Gate stack	$Ge/SiO_2/HfO_2$	
Metal gate	TiN	
EOT (nm)	1.9	1.7
H_{fin} (nm)	30	
W_{fin} (nm)	20 and 100	
L (nm)	200; 300; 500 and 1000	
Fin	4 (parallel)	

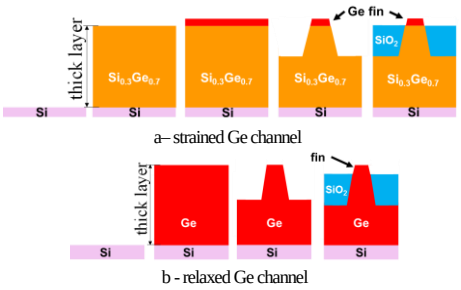

Figure 1. STI last process substrate schematics for relaxed and strained Ge pFinFETs.

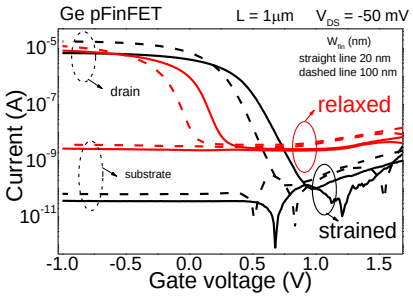

Figure 2. Drain and substrate currents as a function of gate voltage for relaxed and strained Ge pFinFETs.

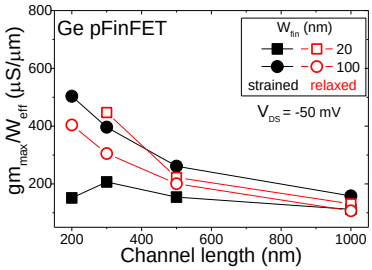

Figure 3. Normalized transconductance as a function of channel length for relaxed and strained Ge pFinFETs in the linear region.

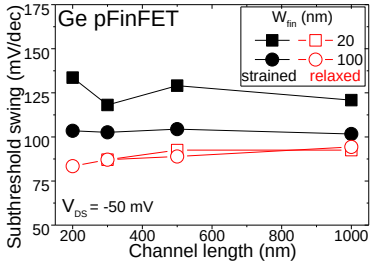

Figure 4. Subthreshold swing as a function of channel length for relaxed and strained Ge pFinFETs in the linear region.

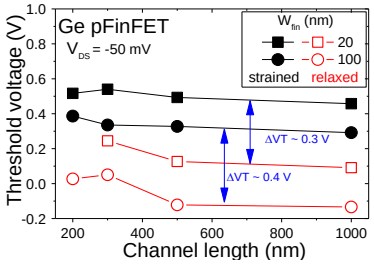

Figure 5. Threshold voltage as a function of channel length for relaxed and strained Ge pFinFETs in the linear region.

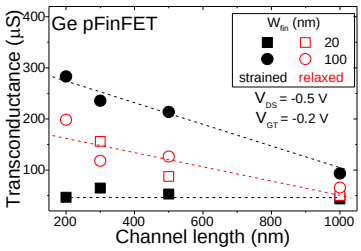

Figure 6. Transconductance as a function of channel length for relaxed and strained Ge pFinFETs in the saturation region.

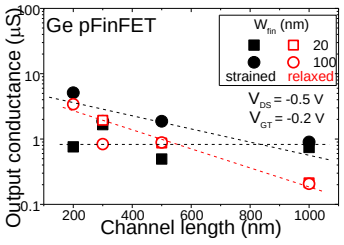

Figure 7. Output conductance as a function of channel length for relaxed and strained Ge pFinFETs in the saturation region.

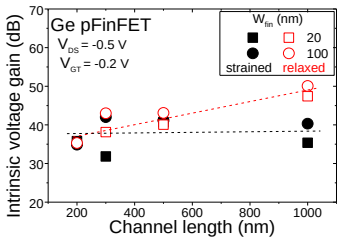

Figure 8. Intrinsic voltage gain as a function of channel length for relaxed and strained Ge pFinFETs.

Layer Thickness Impact on Second Harmonic Generation Characterization of SOI Wafers

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***Abstract* - This paper presents Second Harmonic Generation (SHG) as a non-destructive characterization method for Silicon-On-Insulator (SOI) materials. For thick SOI stacks, the SHG signal is related to thickness variations of the different layers. However in thin SOI films, the comparison between measurements and optical modeling suggests a supplementary SHG contribution possibly attributed to the electric fields at the SiO_2/Si interfaces. The impact of this behavior is that the SHG technique could be used to evaluate interfacial electric fields and consequently interface charge density in SOI materials.**

Keywords* - *SHG; SOI; nonlinear optics modeling; multilayers.

I. Introduction

State of the art ultrathin SOI wafers require novel non-destructive characterization techniques for their interfacial quality evaluation before device fabrication. In this context, optical methods are interesting choices due to their nondestructive nature. Second harmonic generation (SHG) has proven to be sensitive to different interfaces in SOI materials [1], [2] due to the centrosymmetric crystal structure of Si. Previous results [3] suggested that the thickness of the Si layer could play a critical role in the SHG response through the absorption of the fundamental and second harmonic (SH) frequencies. To quantify this effect we developed a multilayer optical model including propagation phenomena, as well as absorption in order to explore the SHG technique's potential applications for interface characterization.

II. Layer Thickness and SHG Measurements

SHG measurements were performed using the Harmonic F1x® equipment [4] with a fundamental radiation at 780 nm (SHG at 390 nm). The layer thicknesses were measured on the same spots using a reflectometer integrated in the equipment. Fig. 1a shows a correlation between the Si layer thickness and the SHG signal for a thick SOI wafer with t_{Si} = 145 nm and t_{BOX} = 1000 nm. Fig. 1b was obtained for a thinner SOI (t_{Si}=88 nm and t_{BOX}=145 nm) of 300 mm wafer diameter. The SHG measurements are clearly related to the thickness variations, however the trends obtained on thick and thin SOI look different. The paper analyzes whether the differences between the two SOI structures are solely attributed to multilayer optical propagation effects.

III. Multilayer Optical Model

For explaining the aforementioned SHG results we model the fundamental and second harmonic optical phenomena in the SOI multilayered structure by using a matrix formalism [5]. The nonlinear optical polarization which drives the SH response is added at each interface (Fig. 2) according to [1]:

$$I_{2\omega} \sim \left(P_{2\omega}^{NL}\right)^2 \sim \left|\chi^{(2)} + \chi^{(3)} E_{dc}(t)\right|^2 I_{\omega}^2 \qquad (1)$$

where $\chi^{(2)}$ and $\chi^{(3)}$ are the 2nd and 3rd order nonlinear susceptibilities, respectively. The $\chi^{(2)}$ values used in the model were taken from [6]. The *dc* electric field $E_{dc}(t)$ at the interface is not taken into account because we want to verify whether the optical interferences alone could explain the SHG measurements. In Fig. 2 the 5-layer structure used for the model is depicted, numbered from top (air) to bottom (substrate) along with the boundary conditions used for the electric fields at both wavelengths. The model evaluates the optical electric fields highlighted with circles.

IV. Results and Discussion

In Fig. 3a and Fig. 3b the SHG signal from the measurements (data points from Fig. 1a and 1b) and the model (line) are plotted versus the Si film thickness. The agreement between model and experiment is very good for both SOI stacks. In order to further validate the model we performed SHG at various angles of incidence (AOI) of the fundamental beam. Fig. 4a shows the SHG measurements at two different points on the same wafer. The curves are well reproduced by the model (Fig. 4b); the thickness of Si film and BOX that were used for the simulation were taken from the reflectometry measurements (see Fig. 1a). The strong correlation between experimental and simulated results, which is true for the thick SOI stack, is less convincing for thin SOI substrates. In thin films the model based exclusively on linear optical propagation is limited to explain the experimental results. Indeed in this geometry configuration, the SHG is also highly sensitive to electric field coupling effects between the interfaces [7].

V. Conclusion

A correlation between Si film thickness and SHG behavior was established for thick SOI wafers and verified by an optical multilayer model. In the case of thinner SOI, absorption and optical interference effects are not sufficient to describe the experimental results.

This is actually a highly encouraging result since it validates the interest in SHG for electric field and subsequently interface states characterization.

ACKNOWLEDGMENT

This work is supported by Region Rhône Alpes (ARC6 program). We would also like to thank SOITEC for inspiring discussions.

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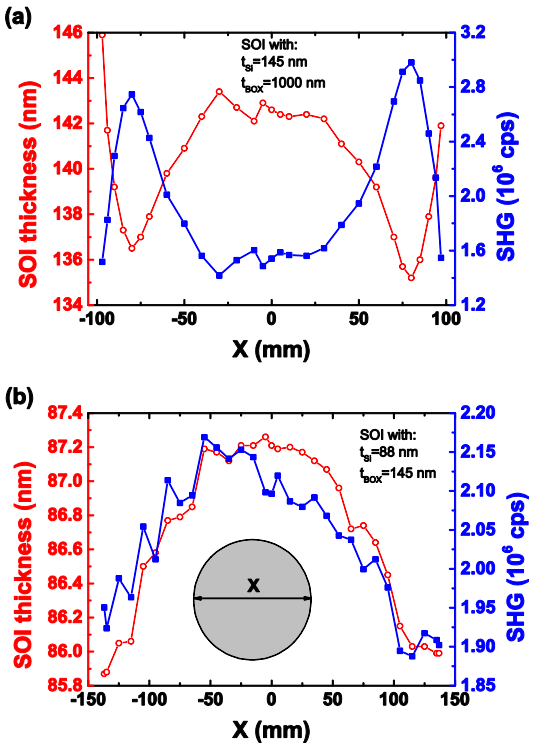

Figure 1: Thick (a) and thin (b) SOI film thickness (open circles) correlation with SHG signal (filled squares). The X-axis in both cases corresponds to different measurement locations on the same wafer (as shown in the inset of Fig. 1b). The angle of incidence was set at 45°.

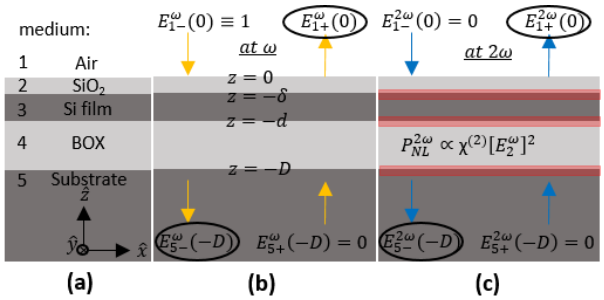

Figure 2: Optical model of the multilayer geometry (a); boundary conditions and calculated fields (in circles) for the fundamental frequency (b) and the SH frequency (c). The nonlinear polarization at each interface is also shown in (c).

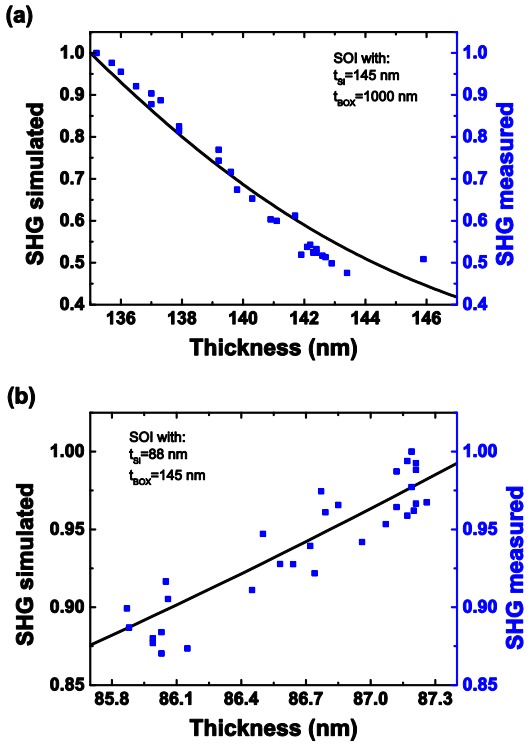

Figure 3: Model (line) and experiment (data points) comparison for thick (a) and thin (b) SOI. The normalized data points were calculated from Fig. 1a and 1b for both cases.

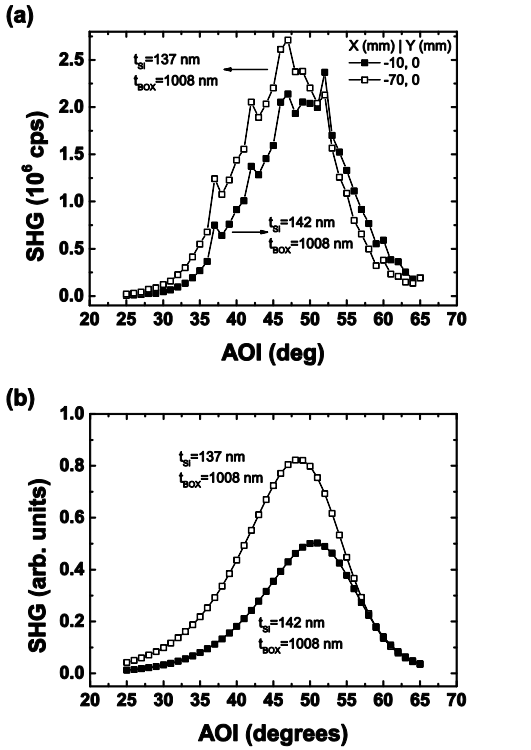

Figure 4: (a) SHG versus angle of incidence measured at two different locations on the same wafer with different Si layer thicknesses (137 nm and 142 nm respectively). (b) Results from the simulation with the only varying parameter being the Si film thickness.

FLEXIBLE PIEZOELECTRIC TRANSDUCERS BASED ON A PMMA/ZNO NANOWIRE COMPOSITE

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***Abstract*— This paper reports on the experimental and theoretical study of flexible piezoelectric transducers with an active area of ~1cm² made of a thin active composite material (~3µm thick) over a thin metallic foil (~25µm of Stainless Steel). The composite material structure is made of vertical piezoelectric nanowires (NWs) embedded into a PMMA dielectric matrix. The open circuit voltage was measured on different devices under manual bending. The performance was evaluated in function of the thickness of the top layer of PMMA in the composite structure of different devices. It was found that the output voltage increased as the thickness of the top layer was reduced. These preliminary results confirm the theoretical FEM simulations and give important guidelines for the optimization of flexible piezoelectric transducers.**

Keywords-ZnO nanowires; piezoelectricity; mechanical energy transducer; FEM simulation

I. INTRODUCTION

Piezoelectric energy transducers have attracted the attention of the scientific community for the last 10 years since the demonstration of energy generated by the deflection of a single ZnO NW [1]. These devices can be used in mechanical sensing applications or mechanical energy harvesting for autonomous systems [2]. Many devices have been reported integrating vertical semiconducting nanowires into a dielectric matrix [3] but not many reports study the optimization of the structural parameters of this composite material. In this paper we report experimental and theoretical results on flexible energy transducers integrating a composite material: ZnO NWs into a PMMA matrix (Fig. 1).

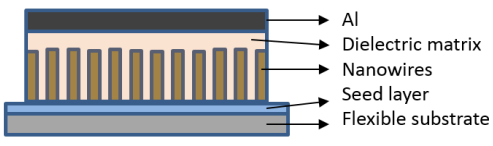

Figure 1. Schematic diagram of the flexible energy transducer integrating a composite piezoelectric material based on ZnO NWs.

In particular we evaluate the effect of the variation of the thickness of the top layer of PMMA on the performance of the transducer.

II. SIMULATION RESULTS

Simulations were made based on previews FEM studies in our group on flexible piezoelectric transducers [4]. A 2D mechanical model of the bending plate is used to calculate the strain in the active layer of the transducer (i.e. composite material) for an input pressure of 100Pa (Fig. 2a). This strain is used as input for a more elaborate 3D model of a unit cell of the composite material (Fig. 2b). This model considers ZnO NWs 600nm long and 50nm in diameter with a cell width of 100nm. The

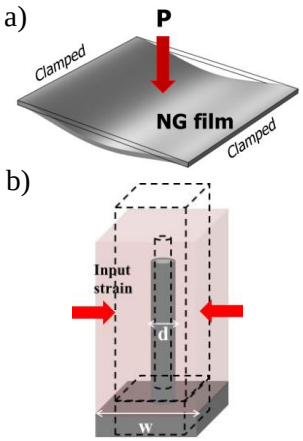

Figure 2. Schematic of the modeling procedure. a) a model of a plate under bending was first used to calculate the strain at the active part (composite material). b) The strain from the plate model is used as input for the multiphysic model of a single cell of the composite material.

voltage generated from this cell with a variating top layer PMMA thickness from 0.1µm to 2.5µm is shown in Fig. 3. A clear trend can be seen, a thinner layer would improve the electric potential generated.

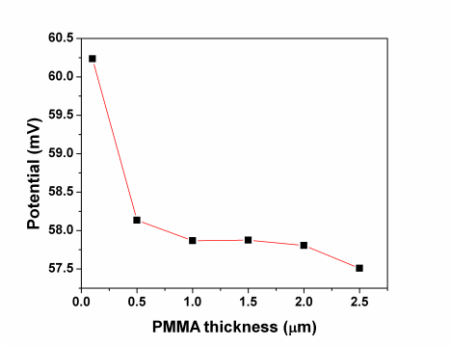

Figure 3. FEM simulation results. Potential generated in fonction of the thickness of the top PMMA layer of the composite material.

III. DEVICE PREPARATION

Piezoelectric ZnO NWs were grown using hydrothermal method on flexible stainless steel substrate with Atomic Layer Deposition (ALD) coated ZnO seed layer. Scanning electron microscopy (SEM) analysis shows the well-aligned ZnO nanowires grown with a diameter of 200±50 nm and length of 3.5±0.3 µm (Fig. 4). This was followed by dielectric material deposition as a matrix material. The dielectric material provides structural stability to nanowires and improves the overall life time of the device. The PMMA matrix layer was deposited by spin coating, it consist of a double coating of 495 PMMA A2 and A6 resists. The thickness of the top layer of PMMA was varied from about 1µm to 2.5µm. Aluminium (200nm) was deposited as top electrode over the dielectric matrix by evaporation.

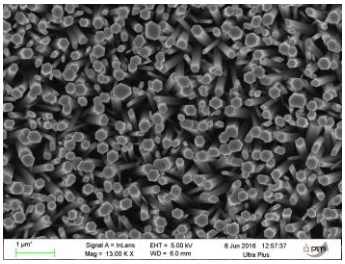

Figure 4. SEM image of the vertically grown ZnO NWs

IV. RESULTS AND DISCUSION

After fabricating the NG devices, the generated voltage under manual bending (estimated bending of 0.5cm) were recorded, observed and analyzed. The open-circuit voltage output decreased as the thickness of the top layer of PMMA increased (Fig 5 and 6). A device having a 1µm thick top layer of PMMA will provides about 4 times more potential (~160mV) compared to a device with thicker layer (2.5µm). The experimental results are in agreement with the theoretical trends provided by FEM simulations (Fig. 3).

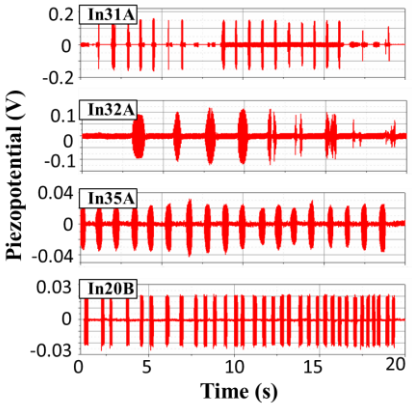

Figure 5. Potential generated vs. time from different samples as they are manually bent about 0.5cm.

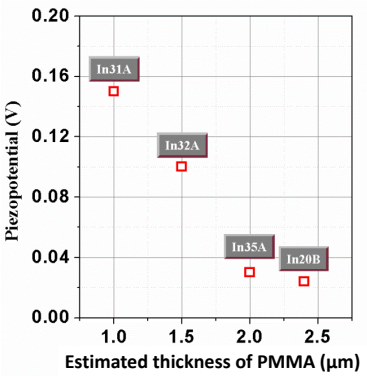

Figure 6. Maximum potential generated for different samples in function of their top PMMA layer thickness.

ACKNOWLEDGMENT

This work has been performed with the help of the "Plateforme Technologique Amont" from Grenoble, with the financial support of the "Nanosciences aux limites de la Nanoélectronique" Fundation and CNRS Renatech network. This work is also supported by funding from the national Nano2017 project.

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Analog parameters on pMOS SOI Ω-gate nanowire down to 10 nm width for different back gate bias

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***Abstract*—This paper shows for the first time, the influence of back gate bias (V_B) in some analog parameters on pMOS Silicon-On-Insulator (SOI) omega-gate nanowire (ΩG-NW) devices down to 10 nm width (W). An excellent electrostatic control is observed in devices down to 40 nm of channel length. The saturated transconductance slightly increase while the output conductance slightly decrease with V_B increment, resulting in an increase of intrinsic voltage gain (A_V) up to 30% for wider devices.**

Keywords: SOI; Omega-Gate; Nanowire; Back gate; p-type

I. INTRODUCTION

The Silicon-on-Insulator technology enables the downscaling of the transistors, as is a request for the continuity of MOSFET roadmap. The geometry of the transistors has been developed along the years and the nanowire (NW) gate-all-around (GAA) transistors are options widely studied options by the scientific community. The main proposal of the GAA structure is to maximize electrostatic gate control, however this requires a high level of complexity in manufacturing.

In order to reduce manufacturing complexity and maximize the electrostatic confinement is used an SOI (Silicon-On-Insulator) Ω-gate nanowire [1-4]. It has already studied and demonstrated the performance of NW with respect to strain on mobility [5-9], low-frequency noise [10, 11], crystallographic orientation [7, 10, 11], and scalability effects [1, 5, 12].

The study of the dependence of back gate bias was done in [13] for nMOS Ω-gate nanowire devices.

This work presents the first analysis of dependence of back gate bias on pMOS Ω-gate nanowire devices. This work presents the analysis of influence of back gate bias (V_B) on the threshold voltage, subthreshold swing and also some analog parameters for different devices dimensions.

II. DEVICE CHARACTERISTICS

The pMOS SOI Ω-Gate NW transistors studied in this paper were fabricated at CEA-LETI. They have a 145 nm of buried oxide thickness on (100) SOI wafers. The gate stack is composed by HfSiON/TiN (EOT=1.3nm) and the silicon height (H_{NW}) is 11 nm. More details about the fabrication of these devices can be obtained in [1]. The devices studied have the gate width ranging from 220nm down to 10 nm and the channel length from 200 nm down to 10 nm. However, to analyze the back gate bias influence without the short channel effect (SCE) the channel length of 40 nm was chosen in specific cases.

Fig. 1 shows the SEM and cross sectional TEM images of the device [1]. There is only one difference comparing the conventional trigate and this device, which is the H_2 anneal used to round the NW [1].

III. RESULTS AND ANALYSIS

Fig.2 shows the drain current as function of front gate bias to different back gate bias of pMOS Ω-Gate NW for wide (220nm) and narrow (10nm) widths. It is possible to note that the narrow channel has less influence of the back gate bias comparing to the wider channel as expected. This effect occurs due to the better electrostatic control between gate and channel in narrow channel. Besides that, the wider channel is a quasi-planar UTB SOI MOSFETs [13].

The threshold voltages (V_T) and the subthreshold swing (SS) as a function of the transistor channel length (L) for different channel widths are illustrated in fig. 3. For all channel width, the electrostatic control is keeping well down to 40 nm gate length .

In order to avoid the SCE in all devices that have been studied and considering that we intend to study the back bias influence on SOI Ω-Gate NW transistors the results (in the next figures) are only shown for L = 40 nm.

The V_T as a function of V_B are illustrated in Fig. 4. As show in fig. 2 devices with narrows channel has better electrostatic control between gate and channel, therefore the V_T of these devices has less dependence on V_B as shown in fig. 4. For Wider devices and negative back gate bias, the back interface tends to inversion increasing the threshold voltage.

Fig. 5 shows the saturated transconductance (gm_{sat}) and the output conductance (g_{Dsat}) as a function of back gate bias. It is possible to see a slightly improve of both parameters (increase of gm_{sat} and decrease of g_{Dsat}) for positive back gate bias, thanks to better electrostatic coupling.

Fig 6 shows the intrinsic voltage gain for different channel length and gate width. It is possible to see that in general the Av increases for positive back gate bias, up to 30% for wider fins.

IV. CONCLUSIONS

This work presents an experimental study on the back gate impact on some digital and analog parameters extracted from pMOS SOI Ω-Gate nanowire (NW) devices with different channels widths (from 220 nm down to 10 nm). The results show that the smaller height channel provides an excellent electrostatic control in all devices studied down to 40nm channel length. The analog parameters like gm_{SAT}, and g_D are only slightly improve with V_B with results in an increase of A_V up to 30% for wider fins.

ACKNOWLEDGMENT

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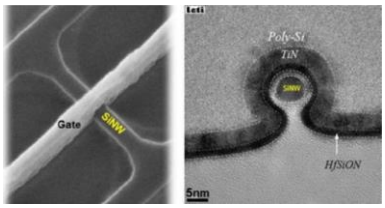

Figure 1: (Left) SEM and (right) cross-sectional TEM images of SOI Omega-Gate Nanowire [1].

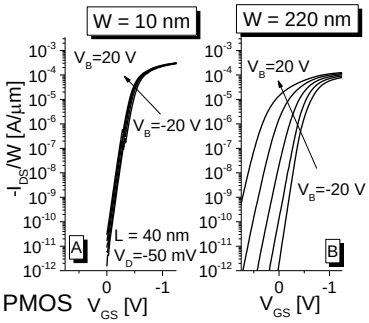

Figure 2: Normalized drain current of Ω-Gate NW for channel width of 10 nm (A) and 220 nm (B) and different back gate bias (V_B).

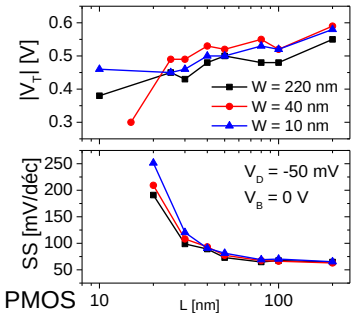

Figure 3: Threshold voltage and Subthreshold Swing of Ω-Gate NW for different dimensions

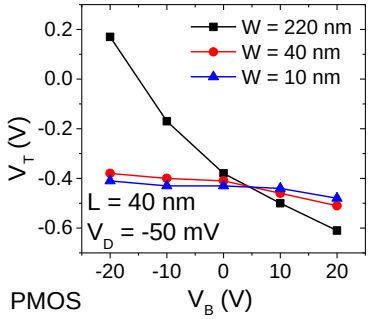

Figure 4: Threshold voltage as a function of back gate bias for different channels widths.

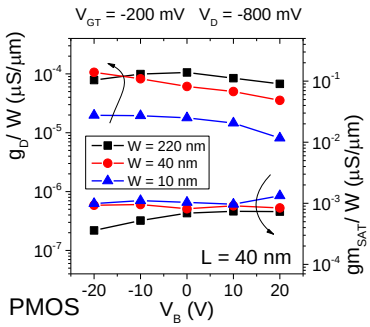

Figure 5: Normalized output conductance (g_D) and transconductance at saturation region (gm_{sat}) as a function back gate bias for different channels widths.

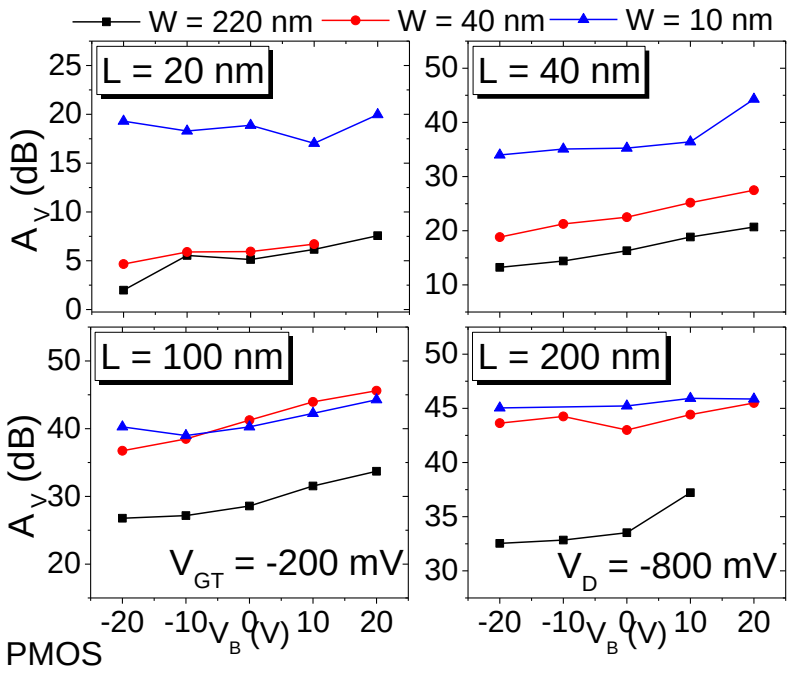

Figure 6: Intrinsic voltage gain (A_V) as a function of V_B for different channel lengths and channel widths.

Quantum Confined Model for a Novel Tri-Material Gate Stack Engineered Double Gate MOSFET

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***Abstract*— The purpose of this research effort is to develop a numerical model for a novel tri-material, gate stack engineered double gate MOSFET considering quantum confinement. While developing this model a combination of 2-D Poisson's equation and 1-D Schrodinger equation was used to obtain the potential profile and inversion charge across the complete silicon film. The proposed DG MOSFET structure has been implemented using Silvaco Atlas 2-D numerical device simulator to obtain the results for transfer characteristics, output characteristics and mobility variation. The results obtained indicate a trend of reduction in mobility and drain current while considering the quantum confined model of the device in comparison to the classical one.**

Keywords- Double Gate MOSFET, Gate Stack, Hetero Gate, Short Channel Effects (SCEs), Volume Inversion.

I. INTRODUCTION

Double Gate (DG) MOSFETs have been making their way in technology circuits since last many years [1-7]. Inspite of their many advantages like low subthreshold leakage, high I_{ON}/I_{OFF}, an ideal 60 mv/decade slope etc., these devices still struggle to perform well in nanometre scale [1]. Various models have been proposed to take into account the effect of prodigious short channel effects (SCEs) [2-4]. While developing these models, different configuration of device techniques such as making use of high-k dielectrics [2], hetero-gate [3], gate stack engineering [4] etc. have been considered by different researchers. Most of these configurations suffer from one or the other technology issues and hence their use still remains limited. While the performance of DG MOSFETs with high K dielectric gets constrained due to undesirable increase in I_{on}/I_{off} ratio [2], the gate stack engineered device often results in establishing a trade-off between equivalent oxide thickness (EOT) scaling and mobility [4].

In this paper, we propose a novel DG MOSFET structure which harnesses the benefits of both hetero-gate and gate stack engineering. While hetero-gate structures improve both the 'on' and 'off' state characteristics of the device simultaneously [2], gate stack aids minimizing quantum tunnelling [4]. A mathematical model has also been developed to obtain potential profile and inversion charge across the complete silicon film. In addition to it, a comparison has been drawn between the transfer characteristics, output characteristics and mobility values of classical and quantum confined model.

The structure of the paper is as follows: Section II presents the 2D cross sectional view of the device, parameters and simulation models. Analytical model formulation has been discussed in section III. Section IV discusses the derived results and finally section V provides the conclusion of the research effort and a hint of the detailed work to be made part of the full paper to be submitted later for this conference.

II. DEVICE STRUCTURE

The implemented device structure is shown in Fig. 1. The device parameters along with their values used in analysis are as follows: Channel length under gates M1,M2,M3=10nm, work function of metal M1=4.69eV, M2==4.29eV, M3=4.19eV, EOT=1.1nm, source and drain doping (n^+) $=10^{20}/cm^3$ and channel doping (lightly p type) $=10^{16}/cm^3$. All simulations have been performed using Silvaco Atlas device simulator.

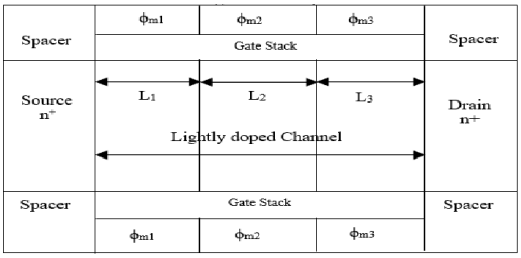

Figure 1. 2D cross sectional view of proposed DGMOSFET.

III. MODEL FORMULATION

Before the onset of strong inversion, potential across the silicon film in 2D is given by Poisson's equation and by using the same parabolic profile given by Young [5] in y direction we get-

$$\frac{d^2\phi(x,y)}{dx^2}+\frac{d^2\phi(x,y)}{dy^2}=\frac{qN_A}{\varepsilon_{si}} \quad ...(1)$$

$$\phi_i(x,y)=a_i(x)+b_i(x)\cdot y+c_i(x)\cdot y^2 \quad ...(2) \ \textit{where}\ 1\le i\le 3\ \textit{for metal gates}\ 1,2\ \textit{and}\ 3$$

We have included few more boundary conditions as stated below in addition to the work already done by Young [5].

$$\phi_1(0,0)=V_{bi}$$

$$\phi_3(L_1+L_2+L_3,0)=V_{DS}+V_{bi}$$

$$\phi_1(L_1,0)=\phi_2(L_1,0)$$

$$\phi_2(L_2,0)=\phi_3(L_2,0)$$

$$\left.\frac{d\phi_1}{dx}\right|_{x=L_1}=\left.\frac{d\phi_2}{dx}\right|_{x=L_1}$$

$$\left.\frac{d\phi_2}{dx}\right|_{x=L_2}=\left.\frac{d\phi_3}{dx}\right|_{x=L_2}$$

Solving equations 1 and 2, we get equation 3 whose solution is given by equations 4,5 and 6.

$$\frac{d^2\phi_{f_i}(x)}{dx^2} - \alpha\phi_{f_i}(x) = \beta_i \ldots(3)$$

$$where\ \alpha = \frac{2\left[1+\frac{c_f}{c_{si}}+\frac{c_f}{c_b}\right]}{t_{si}^2\left[1+2\frac{c_{si}}{c_b}\right]}$$

$$and\ \beta_i = \frac{q_{NA}}{\varepsilon_{si}} - \frac{2V'_{sub_i}}{t_{si}^2\left[1+2\frac{c_{si}}{c_b}\right]} - \frac{2V'_{gsi}\left(\frac{c_f}{c_{si}}+\frac{c_f}{c_b}\right)}{t_{si}^2\left[1+2\frac{c_{si}}{c_b}\right]}$$

$$here\ i = 1,2,3$$

$$\phi_{f_1}(x) = C_1 e^{\sqrt{\alpha}x} + C_2 e^{-\sqrt{\alpha}x} - \frac{\beta_1}{\alpha} \ldots(4)$$

$$\phi_{f_2}(x) = C_3 e^{\sqrt{\alpha}(x-L_1)} + C_4 e^{-\sqrt{\alpha}(x-L_1)} - \frac{\beta_2}{\alpha} \ldots(5)$$

$$\phi_{f_3}(x) = C_5 e^{\sqrt{\alpha}(x-L_1-L_2)} + C_6 e^{-\sqrt{\alpha}(x-L_1-L_2)} - \frac{\beta_3}{\alpha} \ldots(6)$$

Plotting 4, 5 and 6 using Silvaco Atlas yield the complete potential profile across the film. Solving 1D Schrodinger equation for 3 rectangular potential wells within the structure as Naskar et al. [6] gives inversion charge across the film.

$$Q_{inv,q} = \frac{qkT}{\pi\hbar^2} [\sqrt{m_l^* m_t^*} g_t \ln \sum_i \times \left[1+\exp(-\frac{1}{V_t}(E_l^{-i} - \phi_{fi}(x) + E_F(x)))\right] + m_t^* g_l \ln\left[1+\exp(-\frac{1}{V_t}(E_l^{-i} - \phi_{fi}(x) + E_F(x)))\right] \ldots(7)$$

2D Poisson's equation and 1D Schrodinger equation are then solved self-consistently to obtain a convergent solution.

IV. RESULTS AND DISCUSSION

Starting with Poisson's equation as indicated in 1 we have elaborated various steps involved so as to reach on to end result in terms of a mathematical equation for potential across the film (eq.4,5,6) and inversion charge (eq.7). Work already cited in literature ([1]-[6]) has been considered as base to develop this mathematical model so as to reach on to final mathematical equation for quantum confined inversion charge.

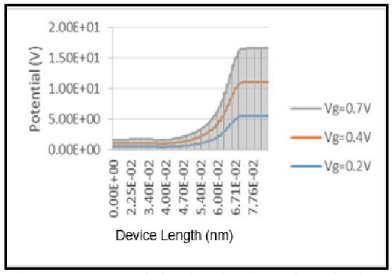

Figure 2. Potential Distribution plot obtained from Silvaco tool while taking into account classical model.

Fig. 2 depicts the potential distribution across the length of the channel for different values of gate voltage (0.2V, 0.4V, 0.7V). The high value of potential close to the drain end of the device is a clear indication of a non-uniform distribution of the potential and is akin to typical FET structures.

The transfer and drain characteristics at Vg=0.7V in fig. 3 and 4 appear to be quiet traditional and in sync with those of a conventional n-channel MOSFET.

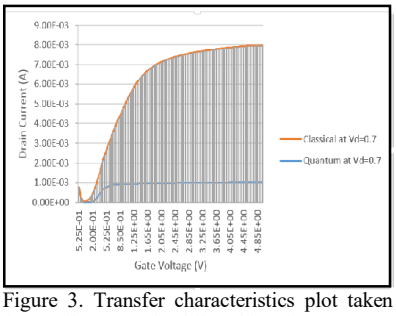

Figure 3. Transfer characteristics plot taken from Silvaco tool while taking into account classical and quantum model.

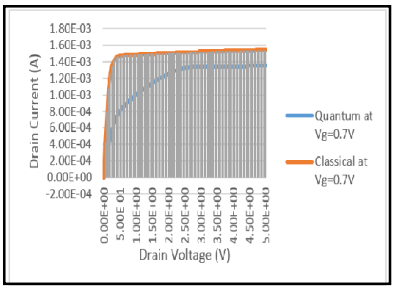

Figure 4. Drain characteristics plot taken from Silvaco tool while taking into account classical and quantum model.

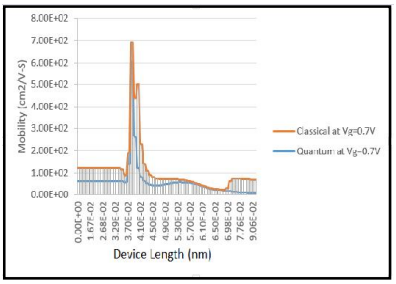

Figure 5. Mobility Variation plot taken from Silvaco tool while taking into account classical and quantum model.

Fig. 5 represents the variation of mobility of carriers across the length of the channel at Vg=0.7V. A spike just at the edge of the gate-source end hints the presence of a wider channel over there. Beyond this spike and close to gate-drain edge of the channel, mobility values are found to be almost constant till the time there is a strong enough pull for the carriers from the drain source potential to enhance these values again. A significant reduction almost of an order of magnitude lesser is observed while having a close look at the plots for the quantum behavior. Davis et al. [7] have explained this behavior earlier while assigning the reduction in degree of freedom and henceforth quantization of carrier energy as the prime reason for the same.

V. CONCLUSION AND FUTURE WORK

1. An analytical model for a novel tri-material, gate stack engineered double gate MOSFET with quantum confinement has been established.
2. The proposed structure with quantum model has been compared to its classical counterpart in terms of transfer characteristics, drain characteristics and mobility variation.
3. Reduction in degree of freedom can be accounted as the chief reason for trend of reduction in values of mobility and drain current obtained from quantum model as compared to classical model.
4. However, in the final version of the paper, detailed model as well as the results and discussions will be presented for the plots obtained for this proposed novel structure of DG MOSFET.

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Characterization of semiconductor structures using scanning microwave microscopy technique

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***Abstract* — In this work, we have developed a scanning microwave microscopy method and applied it to study several semiconductor samples. To do so, we have used a commercial Atomic Force Microscope (NT-NMDT Integra) to which we have coupled a half wavelength micro-strip line resonator and an Agilent N5242A PNA-X Network Analyzer. The AFM tip is connected at the edge of the microstrip which is connected to the PNA. The reflection coefficient S_{11} is measured as the tip is scanned on the device under test. The variations of the S_{11} parameter are related to the topographical and dielectric properties of the material under the tip.**

Keywords-component; Scanning Microwave Microscopy (SMM); Atomic Force Microscopy (AFM); Nanoscale semiconductors characterization.

I. INTRODUCTION

In scanning microwave microscopy (SMM), a performance network analyzer (PNA) continuously feeds the conductive tip of an atomic force microscope (AFM). Depending on the impedance of the tip-sample interface, part of the microwave signal is reflected and measured by the PNA as the reflection coefficient, S_{11}. In SMM, the sample consists of the AFM probe and the region of the device under test immediately beneath the AFM probe tip. The S_{11} parameter depends on the dielectric properties of this region, and therefore the high spatial resolution of the AFM allows us to non-destructively characterize semiconductor structures with high sensitivity and with nanometer resolution, evaluating for example the quality of the interfaces, thickness variations, doping, carrier concentration, etc. [1].

Several commercial SMM solutions are already available. However, in this work we have developed a homemade adaptation to easily convert a commercial AFM in a SMM device. To do so, we have coupled a λ/2 micro-strip resonator to a commercial AFM (NT-MDT Integra) by adapting a specific tip holder. The conductive tip (n-doped silicon tip coated with gold) is connected at the edge of the micro-strip in contact with the conductive line. (Figure 1 and Figure 2). Our device under test consists in a silicon sample, covered with 300nm of SiO_2. Different patterns of gold and aluminum with different sizes and shapes are deposited on top of the oxide. This structure is used to calibrate the system (Figure 3). Figure 3 also shows a AFM image of a gold ribbon on top of the SiO_2. The thickness of the gold metallization is 60-70nm.

II. METHODS AND SETUP

Figure 1 shows a scheme of the setup used and Figure 2 shows some photos of the microstrip and the final setup.

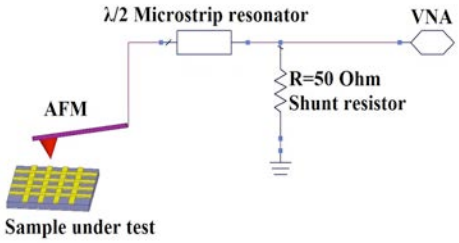

Figure 1. Simplified schematics of the experimental setup

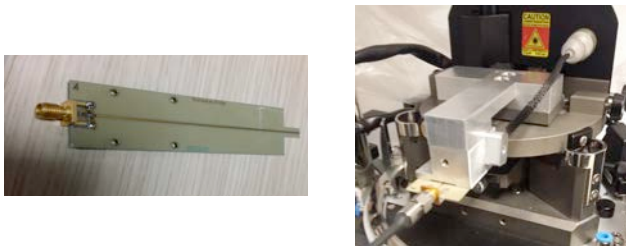

Figure 2. Microstrip (left). SMM-AFM combined system (right).

Once the microstrip is couple to the AFM with a specific holder, the conductive probe tip is placed in contact with the edge of the microstrip, and the latter is connected to the PNA (Agilent N5242A PNA-X Network Analyzer) and a frequency sweep is performed typically from 10Mhz to 26.5 GHz. Figure 4 shows the magnitude of the S_{11} parameter as a function of the frequency. The selected fixed frequency for the experimental procedure was 3.3 GHz.

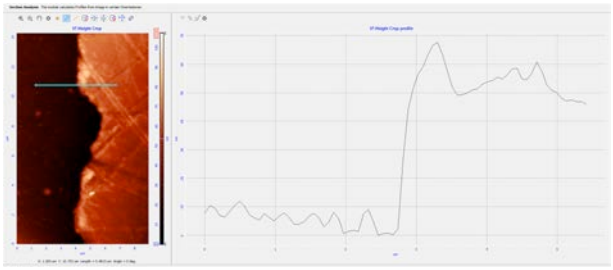

Figure 3. AFM image of the DUT (a), and profile of the Gold metallization (the step is 70nm).

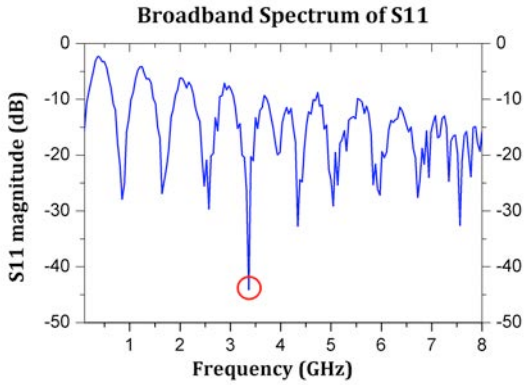

Figure 4. Frequency sweep of the microstrip-tip system. Selected frequency of working (3.3 Ghz)

III Results and Discussion

Once the DUT is placed in the AFM sample holder the tip is approached to the sample and the resonance frequency is recorded as a function of the sample-tip distance over different areas of the sample.

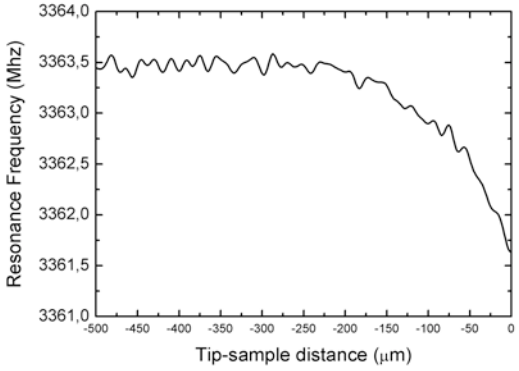

Figure 5. Evolution of the resonance frequency as the tip is approaching the sample.

As the tip is approaching the sample, the resonance frequency of the microstrip remains constant until 150um above the sample. A closer distance from the tip to the sample surface produces a decrease of the resonance frequency, until the contact is produced. The magnitude of the S_{11} parameter also decreases as the tip is approaching the surface of the sample, and the value that this parameter gets near and right at the surface strongly depends on the local dielectric characteristics of the semiconductor sample right under the tip.

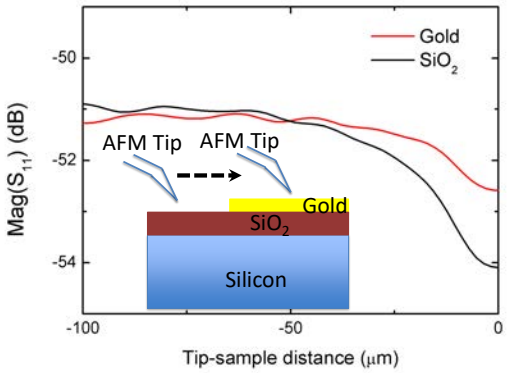

Figure 6. Magnitude of S_{11} as the AFM tip is approaching the surface of the DUT: (red line) the approaching is produced over a point on the gold metallization; (black line) the approaching is produced on the SiO_2 substrate.

Depending on the point where the approach is produced, the value of the reflection coefficient, S_{11}, (shown in Figure 6), the resonance frequency and the quality factor (not shown) of the microstrip are modified. The scanning of the tip on the surface will produce a map of the variations of $|S_{11}|$ on the surface of the DUT, with the spatial resolution that allows the spatial resolution of the AFM. The modifications of these parameters are related to the local properties of the DUT. Although the maximum difference in the $|S_{11}|$ value is produced right at the surface, there is also a noticeable difference hundreds of nanometers above the surface. Therefore, the spatial variation of the properties of the DUT can be detected with this technique without touching the surface, and therefore without producing any defect in the sample. In addition, this technique can also be used to detect changes in the properties of the DUT under the surface, just as doping, carrier concentration, defects, etc..

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Back Enhanced (BE) SOI MOSFET under non-conventional bias conditions

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Abstract –The aim of this work is to investigate the working principle of the new Back Enhanced (BE) SOI MOSFET, under non-conventional bias conditions. This planar BE SOI device with undoped source/drain/channel structure presents the advantage to have very simple fabrication process (without any implantation and electron beam lithography) and can act like a p- or n-type MOS, depending of the back gate bias condition. Under non-conventional bias condition, many electrical parameters present different behavior. The threshold voltage increases linearly with the drain to source voltage (V_{DS}) if $V_{DS} > 0$ and it is constant if $V_{DS}<0$ in case of p-type BE SOI MOSFET. This fact is explained through experimental and simulated data. Special applications will be discussed about this kind of transistors under non-conventional bias conditions.

Keywords — BE SOI, Threshold Voltage; different device architectures.

1. Introduction

The scaling of MOSFET devices faces many technical challenges such as short channel effects (SCE), formation of ultra-shallow junctions and problems related to random dopant fluctuation. New transistor architectures have been proposed to solve these problems, such as the dopant-free nanowire [1]. Another new alternative is the BE (Back Enhanced) SOI MOSFET [2,3], which is an ultra-thin body SOI planar device with undoped source/channel/drain that distinguishes itself by the fabrication simplicity (with no electron beam lithography nor ionic implantation steps). The source and drain are formed by electric field from the back-gate bias and it can operate like a p-type (negative back-gate bias) or n-type (positive back-gate bias) one.

This paper explores the working principle of this new transistor under non-conventional bias conditions using experimental data and numerical simulation results (Synopsys Sentaurus [4]) focus on threshold voltage behavior.

2. Device Characteristics

The BE SOI MOSFET was fabricated at Integrated System Laboratory (LSI) from University of São Paulo (USP), Brazil. It is a planar device made on a SOI wafer with only three conventional photolithography steps and no doping process (there is only the intrinsic wafer doping of 10^{15} cm^{-3}). The final silicon layer and the gate oxide thicknesses are 10nm each. The buried oxide layer thickness is 200nm. The metal gate is aluminum and the drain and source contacts are fabricated with nickel.

The schematic profile of the device can be seen in figure 1 and a picture of transistors array fabricated are illustrated by figure 2.

3. Results and Analysis

As the BE SOI MOSFET is an undoped device, the free conduction charge layer is formed by biasing the back-gate electrode (V_{GB}). When a negative enough V_{GB} is applied, holes are accumulated at the back interface, and therefore, current flows from source to drain when V_{DS} (drain bias) is applied. Thus, one can notice that, differently from a conventional transistor where the drain current flows at the front interface, in the BE SOI MOSFET the drain current flows at the back interface. Similarly, if it is applied a high enough positive V_{GB}, an electron conduction layer is generated at the back interface. Therefore, the BE SOI presents the flexibility of operating as a nMOSFET ($V_{GB}>>0$) or as a pMOSFET ($V_{GB}<<0$).

Figure 3 presents the experimental drain current as a function of the gate bias for a fixed drain voltage and different V_{GB}. One can observe an increase in drain current for higher and positive (n-type) or for lower and negative (p-type) back-gate bias. The increase in the drain current can be explained by the accumulation charges (for $V_{GB}<<0$) or inversion ones (in case of $V_{GB}>>0$) at the back interface. When $|V_{GB}|$ increases, the electric field induced charges also increase at back interface resulting in a higher drain current and a threshold voltage (V_T) variation. Then, figure 3 confirms the BE SOI operation as a pMOSFET or as an nMOSFET depending on the back-gate bias.

The current flow can be controlled by biasing the front-gate electrode. For a BE SOI pMOSFET, if the front-gate voltage V_{GF} is positive enough the silicon layer under the front-gate stack is fully depleted, thus ceasing the current from source to drain. Figure 4 shows the hole density in the silicon layer under the gate electrode (at BB' cross-section, figure 1). For positive front-gate voltage, there is only a small density of holes at the back interface and as the V_{GF} decreases, the density of holes increases until it reaches its maximum value, which is also V_{GB} dependent. From this point, holes are also accumulated at the front interface, where the drain current does not flow, thus they do not contribute much to increase the current. An analogous behavior occurs for BE SOI nMOSFET, but with an electron density accumulation at the back interface instead of holes.

Figure 5 shows the drain current as a function of the front-gate voltage for different V_{DS} values of a BE SOI pMOSFET. It is possible to notice that the current saturates from a certain front-gate voltage where the concentration of holes at the back interface reaches its maximum value. In this situation, the device resembles a resistor and the drain current is proportional to V_{DS}.

Figure 5 also shows a non-conventional V_{DS} bias, i.e., a positive V_{DS} on a BE SOI pMOSFET. The current level differs from positive to negative V_{DS} in the experimental data due to the layout mask used to define the dimensions of the transistor. It defined a common source and six individual drain contacts (figure 2), which can lead to different values for drain and source contact resistances.

A behavior from this fact is that the V_T extracted from the experimental data is approximately constant for negative values of V_{DS} and directly proportional to the drain to source voltage for positive values of V_{DS} (figure 6). This phenomenon can be better understood if we analyze the band diagram in the cross section of the back interface region with different drain to source bias.

Since the hole current flows from source electrode to the drain one in the case of negative V_{DS} value (-100mV, -300mv and -500mV), the energy barrier between source and channel

(h_S) is constant (figure 7). The result is an almost constant V_T. However, if the V_{DS} is positive (100mV and 200mV) the current flows from drain to source and the energy barrier between drain and channel (h_{D1} for V_{DS}=100mV and h_{D2} for V_{DS}=200mV) changes with the V_{DS} variation. As a consequence, the V_T increases for a BE SOI pMOSFET (as shown in figure 6).

The same phenomenon occurs in the BE SOI nMOSFET. If the drain is biased with a positive V_{DS} value (100mV, 300mV and 500mV), the V_T of the transistor remains constant because no variation in the energy barrier between source and channel (h_S) is observed (figure 8). On the other hand, if V_{DS} is negative (-100mV and -200mV) the electron current flows in the opposite direction and the energy barrier between drain and channel (h_{D1} for V_{DS}=-100mV and h_{D2} for V_{DS}=-200mV) varies with V_{DS}, causing a decrease in V_T.

4. Conclusions

This paper explores the behavior of the BE SOI MOSFET under different back gate voltages, source and drain bias conditions. Due to its distinct operation principle, the drain current flows at the back interface and it is possible to have an n- or a p- type transistor in the same device, depending on the back-gate voltage. Moreover, different behaviors were seen depending on the drain to source condition biasing that can assume both positive and negative values unlike conventional MOSFET devices.

The BE SOI MOSFET showed both a flexibility of operation and very simple fabrication process.

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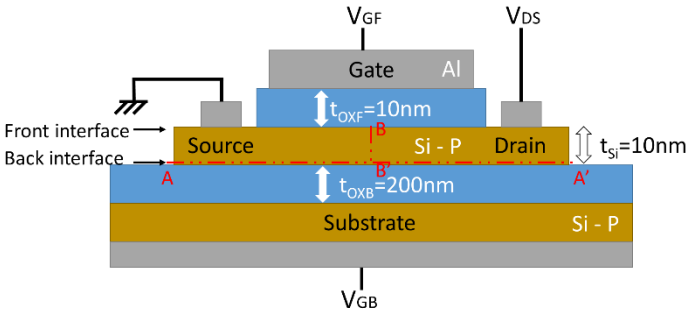

Fig.1 – *BE SOI MOSFET structure.*

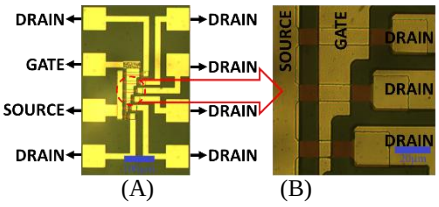

Fig. 2 – *Pictures of BE SOI pMOSFET A) L-array transistors and B) Inset of some transistors fabricated at LSI/USP/Brazil.*

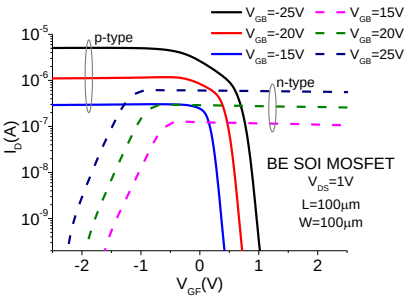

Fig. 3 – *Drain current as a function of the front gate voltage V_{GF}, working like a p-type (V_{GB}<0) and n-type BE SOI (V_{GB}>0)*

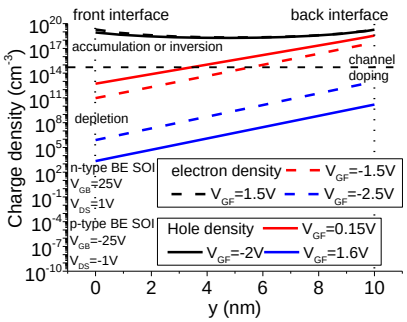

Fig.4 – *BB' Cross section simulation of the charge density for V_{GB}=-25V(BE SOI p-type) and for V_{GB}=+25V(BE SOI n-type)*

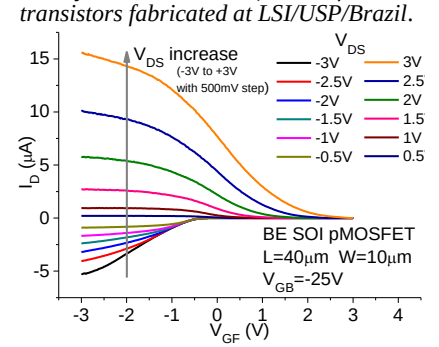

Fig. 5 – *The transfer curves of a BE SOI pMOSFET for different drain bias.*

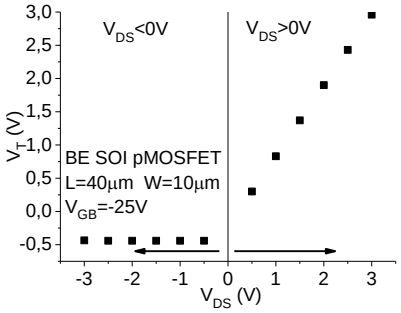

Fig. 6 – *Threshold voltage of the BE SOI pMOSFET as a function of V_{DS}*

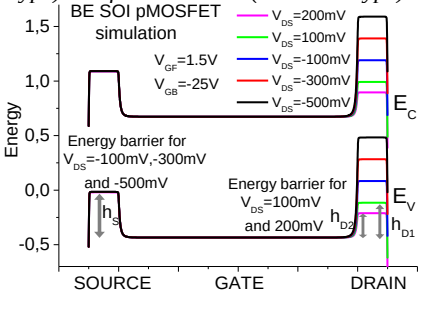

Fig. 7 – *Band diagram simulation of the BE SOI pMOSFET in the AA' cross section for V_{GF}=1.5V, for different V_{DS}*

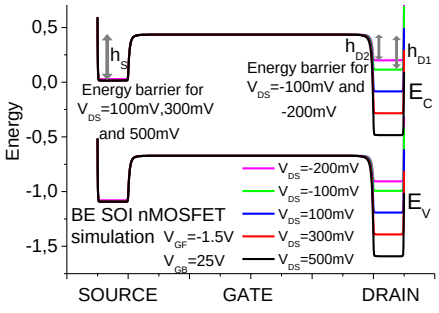

Fig. 8 - *Band diagram simulation of the BE SOI n MOSFETin the AA' cross section for V_{GF}=-1.5V,for different V_{DS}.*

Improved Electrical Characteristics of Gate-Last FD-SOI TFETs with All ALD High-k/Metal Gate Stack Using D_2 Passivation

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***Abstract* — We investigated impacts of D_2 passivation on the electrical characteristics of FD-SOI TFETs with ALD HfO_2 and $HfAlO_x$ gate dielectrics as well as PEALD TiN metal gate electrode. Compared to non-passivated TFETs, higher drive current, improved S.S characteristics, lower threshold voltage and better I_{on}/I_{off} ratio are observed with D_2 passivated HfO_2 or $HfAlO_x$ TFETs. This result indicates that the reduction of interface trap density with D_2 annealing is efficient to reduce S.S characteristics similar to bulk Si FET, which could be an additional process knob to improve interface properties in FD-SOI TFETs**

Keywords – Tunneling FET, HfO_2, $HfAlO_x$, TiN, Deuterium, Passivation, Interface State Density (D_{it})

I. Introduction

The intrinsic thermal limit of the conventional metal-oxide-semiconductor field-effect-transistors (MOSFETs) cannot lower subthreshold swing (S.S) below 60 mV/dec, leading to problems in low power operating. To alleviate the power consumption issue of the scaled MOSFETs, alternative materials and device structure are proposed. Of the emerging devices being investigated, tunneling FET (TFET) has garnered great interest due to the possibility to reduce S.S below the limit (60 mV/dec) of MOSFETs [1-2]. To boost gate capacitance and suppress gate leakage current, high-k gate dielectric (HK) and metal gate (MG) electrode were implemented in MOSFET since 45 nm technology node. Similar to MOSFETs, TFETs with HKMG gate stack were experimentally reported. However, the demonstration of S.S value comparable to or below 60 mV/dec from the HKMG Si-TFETs with acceptable current level is quite limited. This could be due to the intrinsic defects in high-k gate dielectric processed by atomic layer deposition. In addition, interface between high-k gate dielectric and substrate contains some border traps. Therefore, H_2 or D_2 passivation was attempted to suppress interface strap, culprit of S.S degradation. To our knowledge, some preliminary result of D_2 or H_2 passivaion was reported with only N-type Si TETs [3]. In this study, we successfully demonstrated that the characteristics of p-type FD-SOI TFETs with all ALD HKMG gate stack were improved by using D_2 annealing. Regardless of gate dielectrics, improved S.S characteristics are observed with D_2-annealed TFETs.

II. Experiment

6-inch FD-SOI TFETs with both ALD HfO_2 and $HfAlO_x$ with ALD TiN gate were fabricated based on the gate-last process. The SOI wafer was thinned down to 50 nm, followed by active area formation. The S/D regions were implanted by BF_2 and As at 10 keV with dose 3.0 $\times 10^{14}$ cm^{-2}. After S/D activation at 950 ^oC for 5 seconds, HfO_2 and $HfAlO_x$ were prepared by atomic layer deposition at 250-300 ^oC with TEMAHf and TMA precursors, respectively, and H_2O oxidant. The following was 100 nm-thick PEALD TiN with $TiCl_4$ and NH_3 as a precursor and reactant, respectively. Then, subsequent process steps of conventional transistor were processed. The final D_2 annealing was performed at 400 ^oC for 30 minutes under different process pressures.

III. Result and Discussions

Figure 1 shows I_D-V_G characteristics of HfO_2 (a) and $HfAlO_x$ (b) p-type TFETs without and with D_2 passivation, respectively. Compared to non-passivation, improved drain current and lower S.S are attained. It can be attributed to improved interfacial oxide quality and reduced fast trap sites in high-k gate dielectrics. In addition, more enhancements are observed with increasing D_2 annealing pressure. This S.S improvement is substantial with HfO_2 than $HfAlO_x$ while lower I_{off} is obtained with $HfAlO_x$. Figure 2 compares S.S values as a function of D_2 passivation parameters. Clearly, such S.S improvement is dependent of D_2 annealing and process pressure. Figure 3 shows the relation between S.S values and drain current for HfO_2 and $HfAlO_x$ TFETs without and with D_2 anneal. Higher D_2 annealing pressure leads to relative S.S improvement over the wide drain current range for both HfO_2 and $HfAlO_x$. Still, HfO_2 TFET has better S.S stability compared to $HfAlO_x$ TFET as aforementioned. Figure 4 represents V_{th} reduction with D_2 annealing of TFETs with both dielectrics. $HfAlO_x$ TFET has more positive V_{th} shift due

to Al incorporation. However, this shift is independent of annealing pressure. Figure 5 shows I_{on}/I_{off} ratio of HfO_2 (a) and $HfAlO_x$ (b) TFETs, respectively. Both devices shows improved I_{on}/I_{off} ratio with D_2 passivation.

IV. Conclusions

We demonstrated the enhancement of electrical characteristics of D_2 annealed FD-SOI TFET with ALD HfO_2 and $HfAlO_x$ gate dielectric and ALD TiN gate electrode. Compared to non-passivation, improved drain current, lower S.S, reduced V_{th}, and higher I_{on}/I_{off} are obtained with passivation. These improvements are more efficient with HfO_2 than $HfAlO_x$. Our results indicate that D_2 passivation is an additional knob to improve the interface quality of FD-SOI TFET with ALD HKMG gate stack due to the reduction of the trap density.

Acknowledgment

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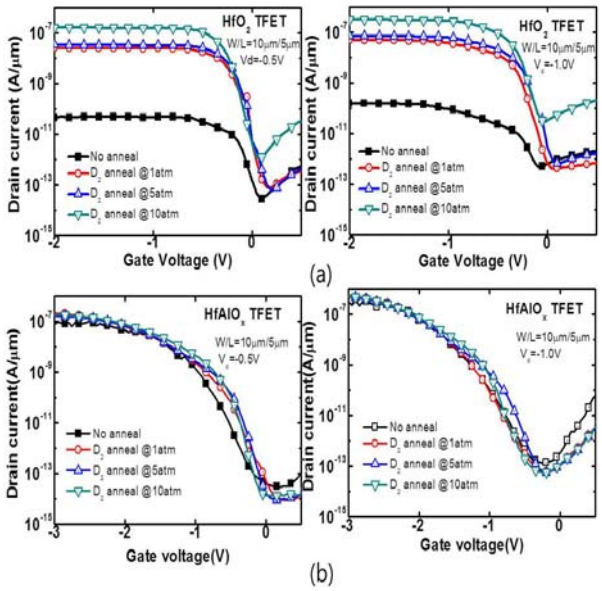

Fig. 1 I_D-V_G characteristics of HfO_2 (a) and $HfAlO_x$ (b) FD-SOI TFET without and with D_2 anneal

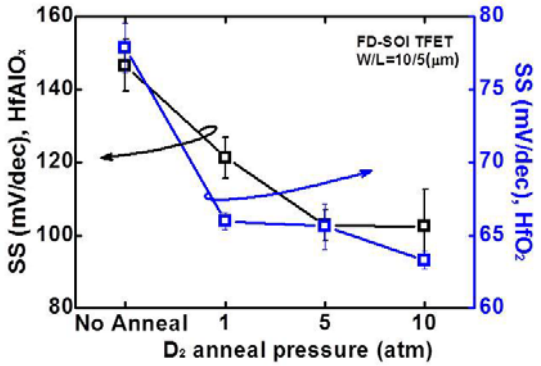

Fig. 2 The S.S values as a function of D_2 annealing process parameters for both HfO_2 (blue) and $HfAlO_x$ (black) FD SOI TFETs

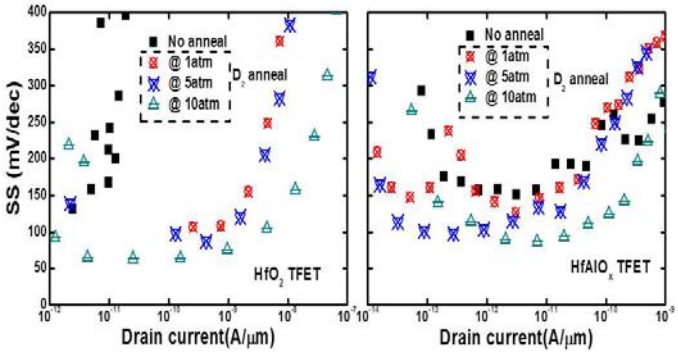

Fig. 3 The S.S values as a function of drain current for both HfO_2 (left) and $HfAlO_x$ (right) FD-SOI TFETs

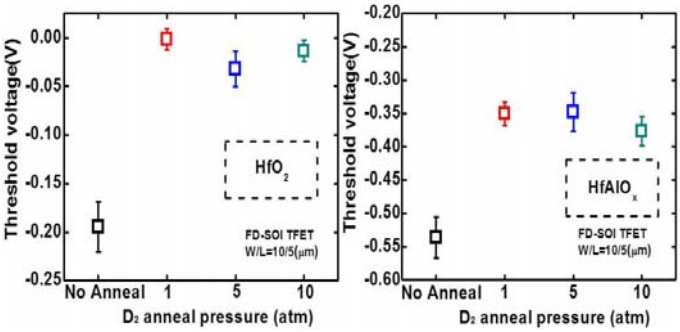

Fig. 4 Threshold voltage as a function of D_2 annealing pressure for both HfO_2 (left) and $HfAlO_x$ (right) FD-SOI TFETs

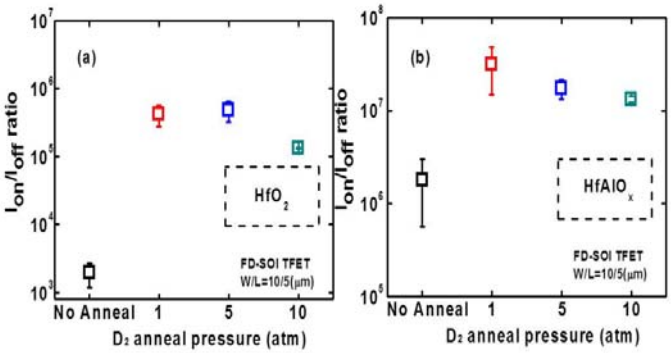

Fig. 5 I_{on}/I_{off} ratio as a function of D_2 annealing pressure for both HfO_2 (a) and $HfAlO_x$ (b) FD-SOI TFETs

A reliable high performance nano SOI MOSFET by considering Quadruple silicon zones

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***Abstract*— A novel nano MOSFET is reported in this paper to achieve high electrical performance. In the proposed structure, 4 silicon zones are considered in the channel and buried oxide. The two N-silicon zones in the channel region create depletion regions that increase the current capability. Moreover, the majority of the holes could be absorbed in these N-silicon regions due to the floating body effect. The two P-silicon zones in the buried oxide help to reduce lattice temperature and creates a way for heat transfer from the active region to the substrate.**

Keywords- MOSFET, SOI, Floating body effect, Maximum lattice temprature.

I. INTRODUCTION

Metal Oxide Semiconductor Field Effect Transistors (MOSFET) are very important in electronic industry for constructing integrated circuits (IC) [1]. However, the trend for achieving the small ICs is a reason for designing small MOSFETs especially in nano scale regime [2, 3]. The performance of MOSFETs can be optimized using Silicon On Insulator (SOI) technology [4, 5]. However, this technology has the famous drawbacks of floating body effect [6] and self-heating effect [7].

In this paper, a new structure for SOI MOSFET in nano scale regime is proposed which can improve the impacts of the floating body effect and the lattice temperature compared to the conventional MOSFET (C-MOSFET). In the new structure, 4 zones are considered which are composed of P type and N type layers. Therefore, the new structure is called Quadruple silicon zones nano MOSFET (QSZ-MOSFET). These zones are considered in the middle of insulator layer and the channel region. The zones have more conductivity than SiO_2. So, the heat can pass through them and the produced holes can go to the substrate. Therefore, the lattice temperature and the floating body effect are improved and more reliable device is obtained which are verified by two-dimensional ATLAS simulator [8].

II. DEVICE STRUCTURE AND MECHANISM

The proposed nano MOSFET structure is shown in Fig. 1. As it is clear in this figure, 4 silicon zones are considered in the channel and buried oxide (BOX). The two N silicon zones are considered in the channel region at the interface of the BOX and have the doping density of 1×10^{15} cm^{-3}. The two P silicon zones are considered in the buried oxide and have the doping density of 1×10^{15} cm^{-3}. The length of the N and P silicon zones are the same and defined as $L_{t\text{-}SZ}$ and the depth of them are defined by $D_{t\text{-}SZ}$ and t_{BOX} symbols, respectively. The channel length is 40 nm and the thickness of silicon on insulator layer is 30 nm. The Length and depth of N silicon zones are 7 nm and 5 nm, respectively. Buried oxide thickness (t_{BOX}) is 20 nm and gate oxide thickness (t_{ox}) is 1 nm. Source/Drain length is 30 nm. Source/Drain doping and Channel doping concentrations are 1×10^{19} cm^{-3} and 1×10^{16} cm^{-3}.

III. RESULTS AND DISCUSSION

In this section, the results of ATLAS simulation are discussed. In Fig. 2 the holes densities of QSZ-MOSFET and C-MOSFET along channel are plotted. The proposed structure has lower holes density in the channel.

For evaluating the reliability of the proposed device, maximum electron temperature in the channel region is plotted in Fig. 3. QSZ-MOSFET has lower electron temperature. This effect is due to the considering N silicon in the channel that causes uniform electric field.

The variation of the lattice temperature in different buried oxide thicknesses is plotted in Fig. 4. In the proposed structure, the heat cannot be transferred from the channel to the substrate due to the down silicon zones which are considered in the buried oxide. So, lower lattice temperature is achieved in the QSZ-MOSFET.

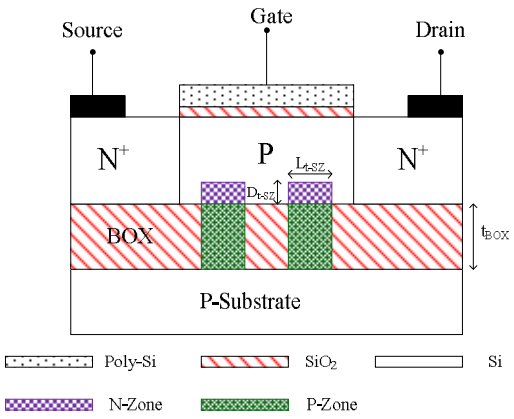

Figure 1. The proposed nano MOSFET structure.

As the temperature increases, the off current enhances in C-MOSFET. As Fig. 5 shows, in the proposed structure due to the reduced lattice temperature, lower off current is achieved. So, the switching capability of the proposed QSZ-MOSFET would be increased.

The higher temperature reduces carrier mobility. As it is clear in Fig. 6, lower lattice temperature of the QSZ-MOSFET causes higher electron mobility in the channel region.

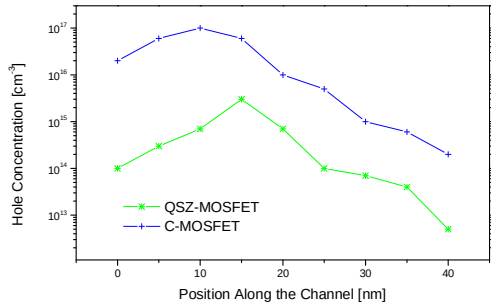

Figure 2. Hole concentration both structures.

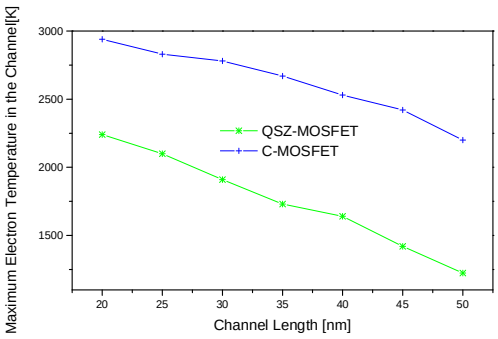

Figure 3. Maximum electron temperature in the channel for both QSZ-MOSFET and C-MOSFET.

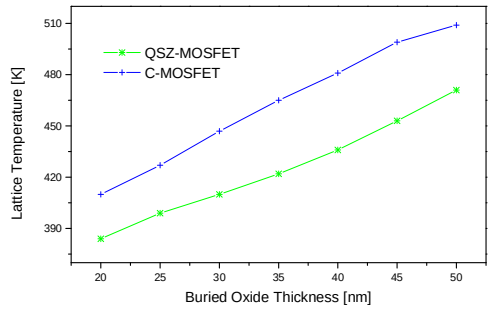

Figure 4. Lattice temperature versus buried oxide thickness for both QSZ-MOSFET and C-MOSFET.

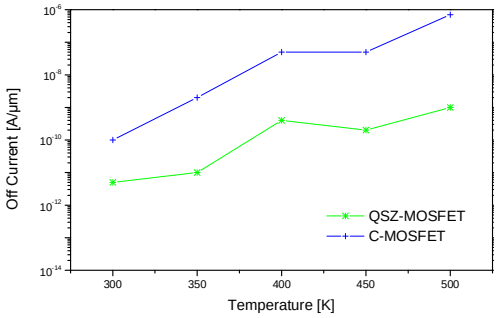

Figure 5. Off current versus temperature for both QSZ-MOSFET and C-MOSFET.

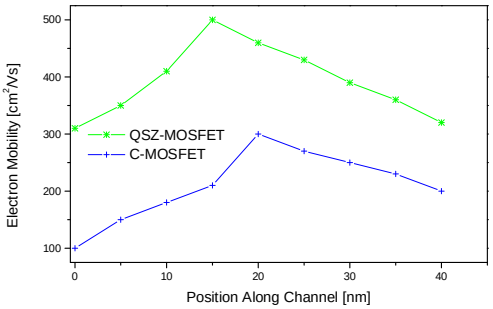

Figure 6. Electron mobility in channel for both QSZ-MOSFET and C-MOSFET.

At the end, by considering the results extracted from ATLAS simulator, it is concluded that the proposed structure has better behavior than the conventional one in case of electrical parameters and it is an acceptable structure.

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Is there a kink effect in FDSOI MOSFETs?

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***Abstract*— Systematic experiments demonstrate the kink effect even in FDSOI MOSFETs. It is the back gate bias which controls the kink effect, via the formation of a back accumulation channel. The kink is more or less pronounced according to the film thickness and channel length. However, in transistors thinner than 10 nm, the kink is totally absent as a consequence of super-coupling effect.**

Keywords- SOI; FDSOI; MOSFET; floating-body effect; kink effect; super-coupling;

I. INTRODUCTION

The kink-effect is a typical floating-body mechanism in partially-depleted SOI MOSFETs: majority carriers generated by impact ionization and stored within the body, lower the threshold voltage [1-3]. The resulting sudden increase in drain current is beneficial for current drive and detrimental for circuit linearity. It is widely believed that FD (Fully Depleted) transistors are kink-free. This myth is inaccurate being contradicted by other floating-body effects demonstrated in FD-SOI (GIFBE, MSD, parasitic bipolar, etc) [4-5]. In this work we investigate the experimental conditions enabling the activation of the kink-effect in state-of-the-art FDSOI MOSFETs.

II. EXPERIMENTAL DETAILS

Several generations of SOI MOSFETs have been examined. The thickness of Si film t_{Si} varied from 25 nm down to 8 nm and the buried oxide (BOX) was 25 nm thick. The fully depleted film was either un-doped ($N_A \sim 10^{15}$ cm^{-3}) or lightly doped ($N_A \sim 10^{17}$ cm^{-3}). The FDSOI process at STMicroelectronics included high-k/metal gate stack with thin or thick dielectric. We probed devices with variable gate length down to L_G = 40 nm. Back-gate bias, -10 V $\leq V_{Gb} \leq$ 0, was applied through a ground plane ($N_A \sim 10^{18}$ cm^{-3}). Five terminal body-contacted devices were also measured for comparison.

III. RESULTS AND DISCUSSION

Fig. 1 shows typical output $I_D(V_D)$ characteristics of 25 nm thick transistor. In normal operation with grounded back-gate (V_{Gb} = 0), there is no kink effect. For negative back-gate bias V_{Gb} = -5V, a marked kink effect develops for $V_D \sim$ 0.7–1V. The kink is accentuated by the interface coupling effect which increases the threshold voltage and lowers the drain current. The amplitude and onset of the kink depend on front-gate bias (Fig. 1), back-gate bias and channel length (Fig. 2). The critical voltage V_C for kink onset is defined as the inflection point in I_D (V_D) curves, in other words the position of the conductance-peak. At constant gate voltage, V_C decreases slightly in shorter devices (Fig. 3) where impact ionization is stronger. However, in very short-channel MOSFETs, the kink is hardly detectable (Fig. 2) for two main reasons: (i) the large output conductance induced by DIBL can mask the kink-related current increase, and (ii) the accumulation of holes is weakened by the proximity of the source and drain junctions. The competition between kink and DIBL is visible in Fig. 4. Remark also that the impact of back-gate bias on kink is attenuated in short devices.

The characteristics of body-contacted MOSFETs with t_{Si} = 25 nm are reproduced in Fig. 5a. Whatever the V_{Gb} bias, there is no kink-effect as long as the body contact is grounded and enable to evacuate the accumulated charge. When the body is floated, the kink occurs for negative V_{Gb}, in agreement with Fig. 1.

The interesting case of ultrathin MOSFET with t_{Si} = 8 nm is shown in Fig. 5b. The key point is that the kink effect cannot be activated by a negative gate bias. This result may look surprising but is actually a direct consequence of the super-coupling effect [6]. Super-coupling forbids the co-existence of electron and hole channels in transistors thinner than ~10 nm. Since the accumulated back-channel cannot be formed, it follows that the front electron channel is kink-free. It is known that in short channels, the super-coupling effect is enhanced and affects thicker devices. This argument can explain the kink-length dependence noted in Fig. 2. The validity of the super-coupling scenario is documented by numerical simulations and dedicated experiments [6].

IV. CONCLUSIONS

Experimental evidence of kink effect in fully-depleted MOSFETs is shown in this work. Kink, super-coupling and back-biasing are inter-related effects. The kink can be activated even in FDSOI films by negative back bias. This is not harmful for circuit because $V_{Gb} < 0$ is used to maintain the transistor in OFF state. In sub-10 nm thick MOSFETs, the kink is impeded by super-coupling.

V. ACKNOWLDDGEMENTS

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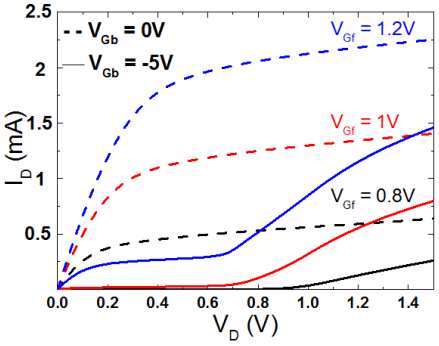

Figure 1. Output $I_D(V_D)$ characteristics with back-gate voltage $V_{Gb} = 0$ and $V_{Gb} = -5$ V. W = 10 µm, L = 150 nm, t_{si} = 25 nm, t_{ox} =2.9 nm, BOX = 25 nm, and doped-body $N_A = 10^{17}$ cm^{-3}.

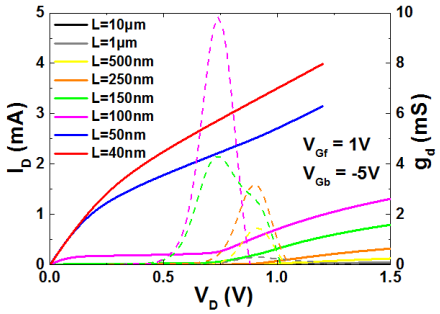

Figure 2. $I_D(V_D)$ and output conductance $g_d(V_D)$ curves for different channel lengths.

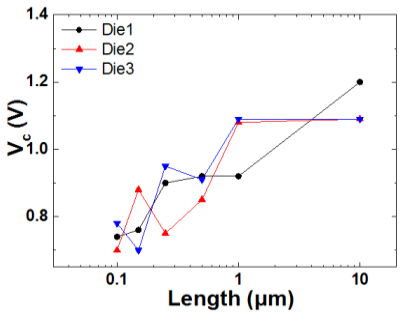

Figure 3. Critical voltage V_c extracted from the peak of output conductance versus channel length.

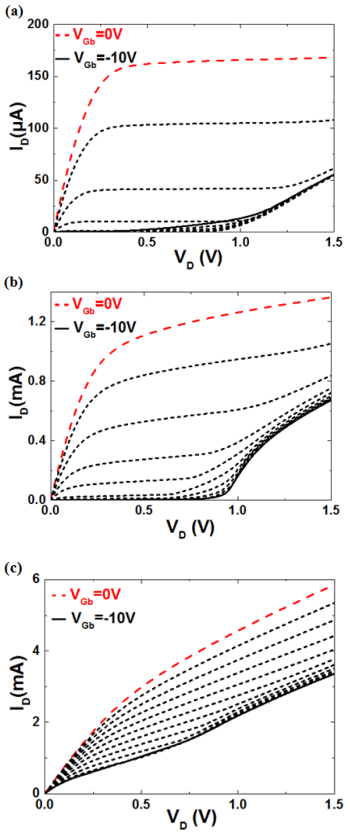

Figure 4. Impact of back-gate bias V_{Gb} from 0V to -10V (step -1V) on $I_D(V_D)$ characteristics for various channel lengths: (a) 1 µm, (b) 150 nm, and (c) 50 nm; t_{si} = 25 nm.

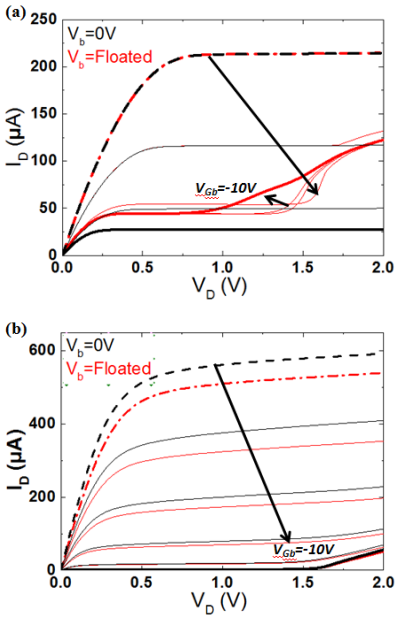

Figure 5. Comparison of $I_D(V_D)$ characteristics of 5-terminal FDSOI MOSFETs measured with the body contact grounded or floated. (a) t_{si} = 25 nm ; (b) t_{si} = 8 nm.

Nanoscale electrical characterization of a varistor-like device fabricated with oxydized CVD graphene

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***Abstract*—The electrical properties of an electron device that contains CVD graphene with oxidized grain boundaries are presented. We found that the device behaves as a varistor, meanwhile AFM analysis confirms the morphology and properties of the oxidized grain boundaries. Because its properties, this device could be used in potential fully-2D materials based circuits.**

Keywords-graphene, photoxidation, varistor

I. INTRODUCTION

Nowadays, the limit of the Moore's Law and the emergence of decentralized technologies like the Internet of Things (IoT) is thrusting the research on alternatives to CMOS technologies to address the new challenges. New materials are being considered, and special attention is devoted to 2D materials due to their unique properties [1]. Graphene, for instance, presents a high electrical conductivity and, at the same time, it is flexible and transparent making it an ideal candidate for its use either in CMOS or flexible electronics. In spite of that, we are still far from the fabrication of a device only with 2D materials without relying on Si technology. For that, 2D counterparts of classical electron devices are needed. In this work, we present and characterize a device fabricated with graphene with intentionally oxidized grain boundaries (OGBs) that behaves as a varistor [2], a key element in electronic circuits.

II. EXPERIMENTAL DETAILS

Two terminal devices were fabricated on top of HfO_2/Si substrates with a 6nm thick oxide layer. Graphene was grown using a chemical vapor deposition (CVD) technique and its grain boundaries were oxidized by means of a photocatalytic oxidation [b]. Then, the resulting graphene layer is transferred onto the HfO_2/Si substrate with the procedure described in [3]. After the transference, a transistor-like device (Fig. 1) is fabricated. The channel of the device is around 60 µm long and 40 µm wide. Due to its similarity to a graphene field-effect transistor (GFET) the current measured will be called drain current (I_d) and the voltage applied drain voltage (V_d). Device level and nanoscale measurements

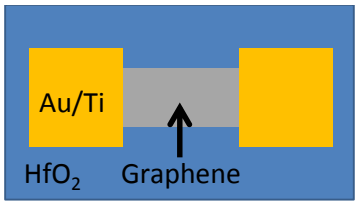

Figure 1. Top view illustration of the device. HfO_2 substrate is presented in blue, electrodes in yellow and graphene in grey.

were performed using a Keithley 4200 Semiconductor Parameter Analyzer and Atomic Force Microscopy (AFM, Nanobserver from Scientec) related techniques, respectively.

III. RESULTS AND DISCUSSION

Device level measurements were performed in order to analyze the lateral conduction (between the two Au/Ti electrodes), I_d, of the devices. Figure 2 presents two representative I_d-V_d curves, measured on two different devices. These curves are radically different from those expected for typical GFETs, which show ohmic behavior [4]. In this case, current is not measured until a threshold voltage is reached. This behavior happens for positive and negative voltages, and the phenomenon is almost symmetrical. This non-ohmic curve resembles to that of a varistor. Also, as can be seen in Figure 2, the device-to-device variability is very high, as we measured devices with a relatively high output current (µA) meanwhile others present current levels of the order of pA. The

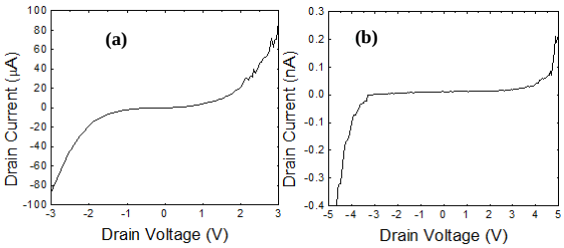

Figure 2. I_d-V_d curves measured on different graphene based varistor devices, showing of (a) high currents and (b) low currents

different behavior compared to a GFET and the high variability could be related to the role of the oxidized graphene GBs. To elucidate the structure of the graphene layer, nanoscale analysis of devices with electrical characteristics similar to those shown in Fig. 2 has been performed with AFM, CAFM and KPFM. Topography images obtained by AFM show the typical structure of CVD graphene but with wider grain boundaries because of their oxidation. Figure 3(a) shows an example measured on a high current device, with the grain boundaries highlighted by using the phase image as a mask. Analyzing various areas of the same device, the mean grain size is estimated to be ≈ 5 μm^2. Topography

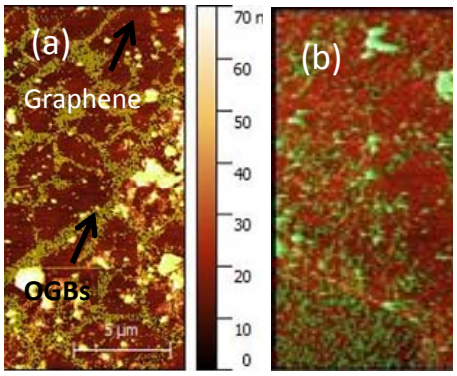

Figure 3. Topography image with the phase contrast image used as a mask in order to highlight the oxydized grain boundaries. (a) High current and (b) low current device

maps of low current devices (Fig. 3(b)) show smaller mean grain sizes (≈2.6 μm^2). Also zones in which the oxidation extends beyond the grain boundaries are observed (Fig. 3b, bottom). So, these results seem to indicate that the oxidized GBs and the percentage of oxidized zones on the global area of the device have a clear impact on the device electrical properties. KPFM and CAFM have also been used to confirm the nature of the different materials detected in the topograhical images (graphene, OGBs and HfO_2). KPFM images (Fig 4) show indeed differences of potential between graphene, OGBs and HfO_2 substrate, with graphene having the higher potential. Around graphene grains, the OGBs can be distinguished over the substrate, which in the KPFM image presents a lower potential than graphene (that corresponds to a different morphology than graphene in the topography image). In CAFM analysis (Fig 5), the topographical image (Fig 5a) shows another graphene region, although this time the OGBs

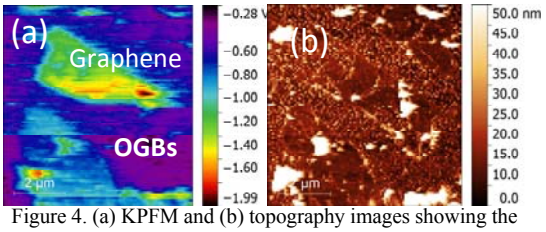

Figure 4. (a) KPFM and (b) topography images showing the differences between graphene (green-yellow) and OBGs (blue-purple)

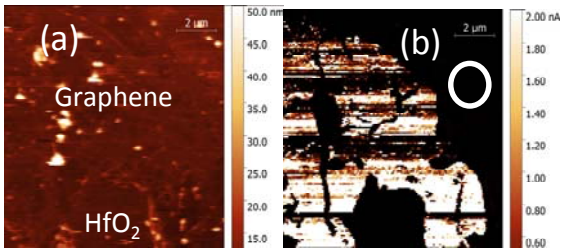

Figure 5. (a) Topography and (b) its current map counterpart highlighting the contrast between HfO_2, graphene and grain boundaries. The circle points a The circle points a degraded area.

are more difficult to be detected because a Pt tip with a larger radius (and, therefore, a worse resolution) was used for the measurement. In this case the HfO_2 substrate is exposed in the lower part of the image. The current image was measured applying a voltage of 5 V to avoid any current through the oxide. When the tip is on the graphene, due to its conductive nature, the contact area will increase, triggering the flow of high current. This behavior is observed in Fig. 5b, where the HfO_2 substrate and grain boundaries (around the graphene layer and inside it) are perfectly defined, confirming that the latter are also nonconductive. Note that a relatively large portion of the layer seems non-conductive, suggesting that in this particular area a part of the graphene layer is degraded.

In conclusion, the electrical and structural properties of a CVD graphene layer with oxidized grain boundaries are studied. We found that because of the oxidation of the grain boundaries, devices fabricated with this material show a varistor behavior, opening the way to their use in fully 2D-material flexible circuits.

ACKNOWLEDGMENT

This work has been partially supported by Spanish MINECO and ERDF (TEC2013-45638-C3-1-R), the Generalitat de Catalunya (2014SGR-384). Qian Wu acknowledges support from the Chinese Scholarship Council (No. 201408390030). B. Sampere and C. Colomines acknowledge the European Social Fund grant for the recruitment of research personnel (2015FI_B200107), IQS – School of Engineering, Universitat Ramon Llull and Flubetech S.L.

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Multi-Subband Ensemble Monte Carlo simulations of scaled GAA MOSFETs.

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***Abstract* — We developed a Multi-Subband Ensemble Monte Carlo simulator for non-planar devices, taking into account two-dimensional quantum confinement. It was employed to study MOS devices based on ultra-scaled Gate-All-Around Si nanowires.**

Keywords: Monte Carlo Simulation; multi-subband; finite elements; mobility; GAA; Si nanowire.

I. Introduction

Non-planar MOS transistors with multiple gates have already entered mass production and represent the most promising solution to the ultimate scaling of CMOS technology. For these devices, the effect of two-dimensional quantum confinement is essential and it is captured in the Multi-Subband Ensemble Monte Carlo (MS-EMC) approach, which, on the other hand, employs the semi-classical Monte Carlo (MC) method to solve the Boltzmann transport equation. In this work, we describe an MS-EMC simulator for 3D devices developed in our group, and show the possibilities it offers by studying the scaling properties of ultimate Gate-All-Around (GAA) MOS transistors with ultra-thin Si nanowires.

II. Simulator description

To simulate a 3D device, we employ the space-mode approach [1], where the Schrödinger Equation (SE) is solved in several cross sections perpendicular to the transport direction. The MC method is employed to simulate the resulting 1D carrier transport in each subband. Self-consistency is achieved by solving the 3D Poisson Equation (PE) in the whole structure. The device is described employing a 3D finite element mesh obtained by extruding a 2D triangular mesh, so that it can be used to discretize the SE in different cross sections. Non-parabolic electron band-structure is taken into account after the solution of the SE by correcting the energy levels and the subband structure as described in [2]. The MC simulation includes carrier scattering by acoustic and optical phonons [3] (taking into account Pauli exclusion principle) and employs a variance reduction technique based on variable super-particle weights depending on energy.

For a given value of the gate bias V_{GS}, the simulation starts with V_{DS}=0 and the non-linear PE is solved with the SE at equilibrium (i.e. employing the Fermi-Dirac distribution) in a predictor-corrector scheme. Then a self-consistent loop including MC, PE and SE is started. In a first stage the boundary conditions at the drain are gradually changed in order to reach the desired value of V_{DS}. After that, the boundary conditions are kept fixed while a self-consistent solution is reached. Finally, the drain current is computed, repeating the self-consistent loop until the required accuracy is achieved. It is also possible to compute the low-field mobility, μ, by a similar procedure. Only the (infinitely long) channel of the device is considered and small values of a uniform electric field are applied in the longitudinal direction. Mobility is extracted by fitting the obtained velocity v.

III. Results

We simulate GAA FET transistors based on cylindrical Si nanowires with channel along the ‹100› direction, diameters ranging from D=4 nm to D=8 nm, gate oxide (SiO_2) thickness T_{ox}=1 nm, undoped channel and midgap

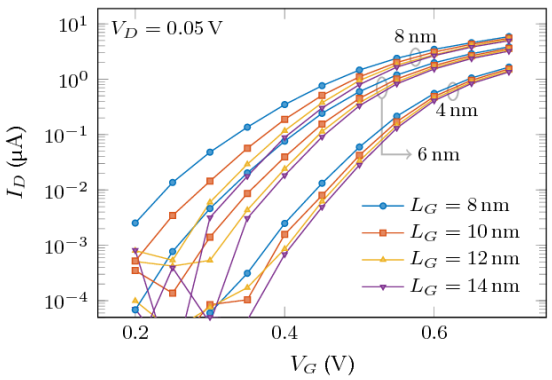

Figure 1. I_D-V_G curves for the simulated devices at V_D=50 mV.

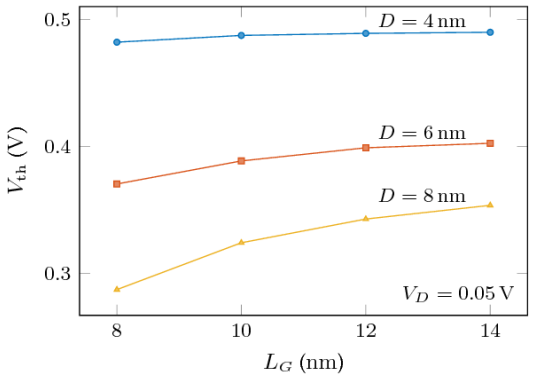

Figure 2. Threshold voltage computed at V_D=50 mV.

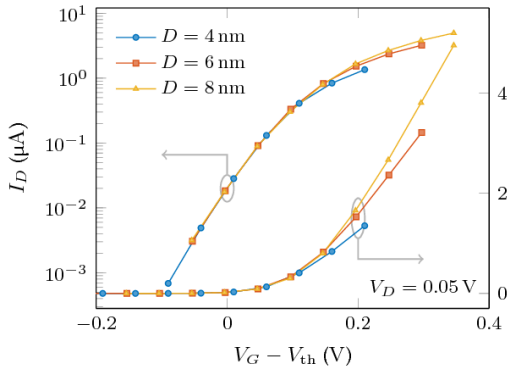

Figure 3. Drain current vs. gate overdrive for L_G=14 nm..

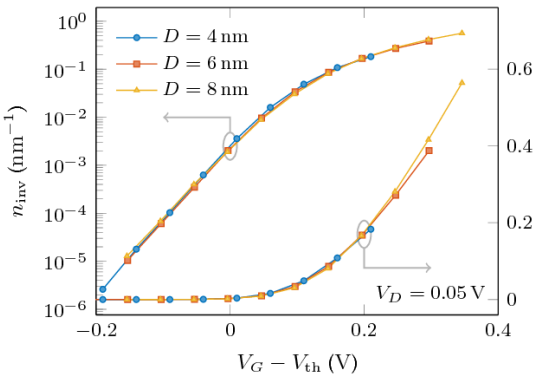

Figure 4. Linear electron density in the middle of the channel.

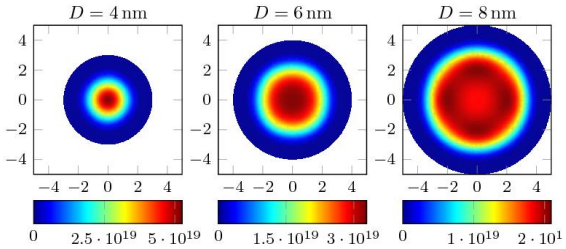

Figure 5. Electron density in the middle of the channel for V_G=0.7 V and different nanowire diameter.

gate work function. Channel lengths L_G from 14 nm down to 8 nm are considered, with S/D doping density N_{SD}=1×10^{20} cm^{-3}, an underlap of L_{sp}=2 nm and Gaussian distribution (σ=0.8 nm). Fig. 1 shows the simulated transfer characteristics: small statistical error is obtained for I_D larger than 1 nA. The threshold voltage, V_{th}, is shown in Fig. 2. Notice how V_{th} is larger for D=4 nm due to quantum confinement with a very small drift with decreasing L_G, while a strong L_G dependence is observed for larger D. If we shift V_G by V_{th}, the I_D-V_G curves corresponding to different values of D (and L_G=14 nm) collapse (Fig. 3) except for the largest applied biases. The curves of the linear electron density n_{inv} near the middle of the channel, collapse in a similar way (Fig 4) and the slight differences at high biases can be explained by the charge distribution shown in Fig. 5. For D=4 nm the peak electron concentration is always located in the center of the cross section, while for wider nanowires peaks can appear along the perimeter for large V_G. The larger discrepancies in

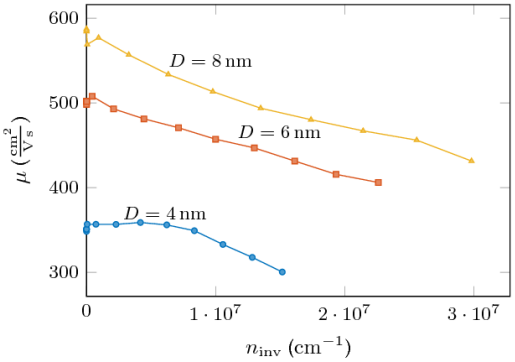

Figure 6. Phonon limited mobility for Si GAA nanowires.

Fig. 3 than in Fig. 4 can be explained taking into account that mobility is severely degraded for decreasing D (Fig. 6). Finally, we computed the DIBL and the subthreshold swing (Fig. 7 and 8), showing that the narrower device with D=4 nm can keep a good control of the short channel effects down to L_G=8 nm.

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The authors acknowledge the financial support of Spanish Government (TEC2014-59730-R) and EU H2020 program (REMINDER, grant agreement No 687931).

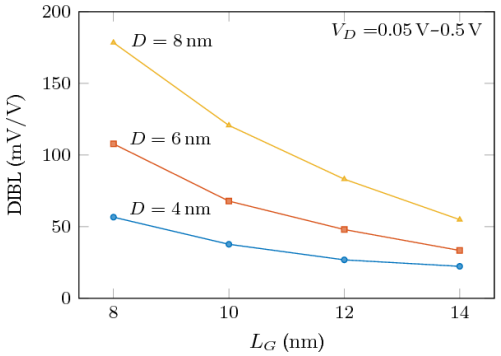

Figure 7. DIBL as a function of the channel length.

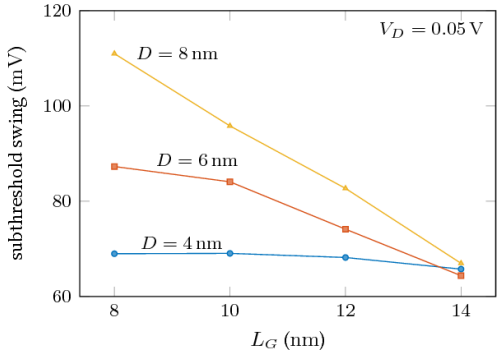

Figure 8. Subthreshold swing as a function of channel length.

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FDSOI MOSFET threshold voltage characterization based on AC simulation and measurements

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***Abstract*— A method for extraction of the threshold voltage corresponding to the front and back interface in FDSOI MOSFETs is proposed. The approach is based on the C-V characteristics of the capacitances between the source and front/back gate. The method has been discussed using the numerical simulation results and has been demonstrated using the C-V characteristics of the experimental FDSOI devices manufactured in ITE.**

Keywords-FDSOI CMOS technology, threshold voltage characterization, C-V measurements, gate-controlled p-i-n diode

I. MOTIVATION

The MOSFET threshold voltage (V_{th}) extraction methods have been derived for the standard bulk-type devices. They have been adapted for characterization of the fully-depleted SOI (FDSOI) technology [1]. These methods face problems related to the small Si film thickness: the effects of the serial resistances and of the mobility degradation at the interfaces on the I-V characteristics, thus on the threshold voltage extraction. Furthermore, the effect of the parasitic current path on the I-V characteristics complicates the V_{th} extraction as well. A simple method to resolve was proposed in [2]. In order to avoid these problems the transconductance-, and capacitance-based methods have been developed. In [3] it has been demonstrated, that the maximum of the $d(g_m/I_D)/dV_G$ characteristics is an improved estimation of the V_{th}. In [4] the gate capacitance (vs anode and cathode tied together) in the gate-controlled p-i-n diode has been used for the V_{th} extraction. In [5] a method based on the C-V measurements of the MOSFET junction capacitance has been proposed. In [4], [5] the current flow effect has been obviously eliminated. In this work we follow [5]. For the extraction of the front/back V_{th} we propose to use the capacitances between the front/back gate and the diffusion area. So, not only the MOSFETs but as well the gate-controlled diodes may be used. Because the available FDSOI MOSFETs were too small for accurate C-V measurements, we demonstrate the method using the FDSOI gate-controlled p-i-n diodes. The proposed approach may be used also for the devices with the doped channel.

II. NUMERICAL MODELING

The method is proposed based on the numerical simulations carried out using Silvaco tools. In the first step ATHENA has been used to simulate the real FDSOI CMOS process transferred from Université Catholique de Louvain (UCL) to ITE. The process is described in the next section. Next, ATLAS has been used for electrical simulations of the C-V characteristics used for the V_{th} extraction. In the simulations the DC current flow was eliminated. In Fig. 1 the electron concentration at the front interface is shown together with the cathode/gate capacitance and its derivative. The characteristics correspond to three different gate and substrate bias conditions. The end of the exponential growth of the electron concentration corresponds to the front gate V_{th} and coincides clearly with the maximum of the $dC_{cathode/gate}/dV_G$. It is worthwhile to note that for the accumulation/inversion at the front/back interfaces two peaks are visible on the $dC_{cathode/gate}/dV_G$ curve. The lower one indicates the V_{th}.

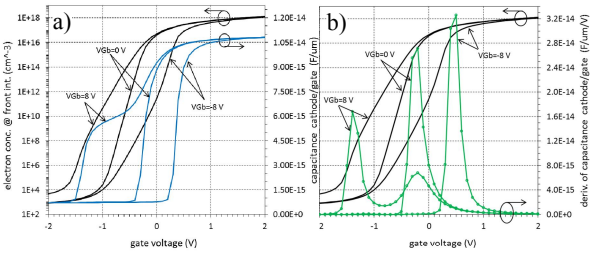

Figure 1. Simulated electron density at the front interface compared with the cathode/gate a) capacitance, b) capacitance derivative.

Analogous simulations have been done for the back

gate threshold voltage characterization. The results are shown in Fig.2. The maxima of the $dC_{cathode/sub}/dV_{sub}$ coincide with the points of the strong inversion onset at the back interface. It is worthwhile to mention that in both cases the capacitance derivative maxima are clearly visible also for the inversion conditions at the opposite interface.

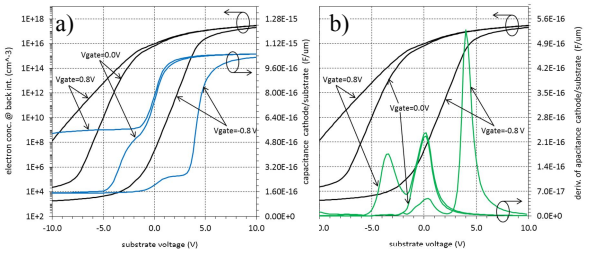

Figure 2. Simulated electron density at the back interface compared with the cathode/substrate a) capacitance, b) capacitance derivative.

The proposed method is illustrated by distributions of the minority carriers for the gate bias ±3V, substrate bias ±8V (Fig.3). According to the varying configurations of the conductive and insulating regions the coupling capacitances appear/disappear. These variations are reflected on the C-V characteristics.

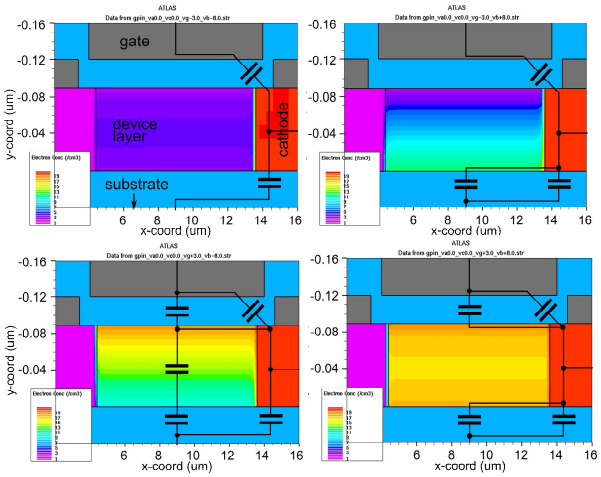

Figure 3. Simulated distributions of electrons in the Si film together with equivalent capacitor networks.

III. EXPERIMENTAL

Using the FDSOI CMOS process, the inversion-mode nMOSFETs and accumulation-mode pMOSFETs with different channel implantation doses were fabricated. The regular MOSFETs have threshold voltages ±0.4 V. The FDSOI CMOS pair is schematically shown in Fig.4. The test MOSFETs were too small for the reliable C-V measurements. So, the gate-controlled p-i-n diodes (chan. length 100µm, width 83µm), shown in Fig.5, were measured. The substrate/cathode C-V characteristics are shown in Fig.6. For the inversion at the back interface they are in agreement with the simulation results (Fig.2a), whereas for the accumulation significant difference is noticeable. We attribute it to the construction of the channel stopper around the active area (Fig.5). The acceptor ions were implanted only along half of the active area edge, close to the n^+ diffusion area. This significantly disturbs the measured $C_{sub/cathode}$. In spite of this parasitic effect the C-V data may be used for the V_{th} extraction.

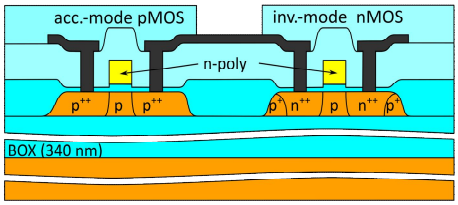

Figure 4. The complementary pair in the FDSOI process.

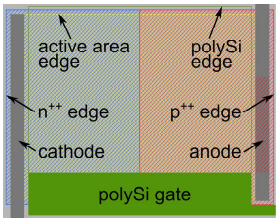

Figure 5. The layout of the gate-controlled p-i-n diode

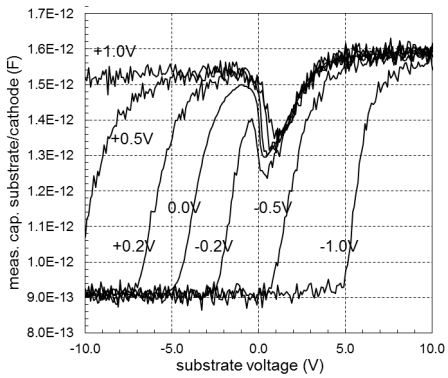

Figure 6. $C_{sub/cathode}(V_{sub})$ characteristics of the p-i-n diode

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Back-gate bias effect on FDSOI MOSFET RF Figures of Merits and Parasitic Elements

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***Abstract*—This work demonstrates that the back gate terminal of a 28nm FDSOI MOSFET can be used up to several tens of GHz for signal processing. Furthermore, the dependence of the main RF figures-of-merit on the back gate bias are experimentally extracted using a 3-port characterization in the frequency range of 10 MHz – 26.5 GHz. We propose a small-signal equivalent circuit constructed based on 3-port measurements allowing for more complete extraction of parasitic elements comparing to the 2-ports one. The effect of back-gate bias on cut-off frequencies is demonstrated and explained in terms of its influence on the relevant parasitic elements.**

Keywords-cut-off frequencies; FDSOI; 3-port S-parameters;

I. INTRODUCTION

FDSOI transistors are widely recognized as a promising candidate to continue downscaling beyond the 28 nm-node for low power and mixed-signal CMOS applications [1]. This technology presents key advantages: Lower variability by using undoped channel [2] and better electrostatic control [3] are amongst the most important improved DC parameters. Moreover, this technology has shown promising RF performances with high current cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) [4]-[5]. One of the most interesting features of this technology is the possibility of back-gate control schemes thanks to ultra-thin buried oxide (BOX) combined with a highly-doped layer underneath the BOX, so called ground-plane (GP), allowing for further improvement of both static and dynamic behaviors of the device [6]. In this work, a 3-ports configuration of FDSOI nMOSFET is employed for extracting the parasitic elements based on an extended small-signal equivalent circuit. The effect of back-gate bias on RF Figures of Merit (FoM) for both front and back gates is investigated and discussed through small-signal equivalent circuit elements.

II. DEVICE AND MEASUREMENT SETUP DESCRIPTION

The studied FDSOI nMOSFET is fabricated in the 28 nm FDSOI platform of ST-Microelectronics [7]. Si body, BOX and equivalent gate oxide thickness are 7 nm, 25 nm and 1.3 nm respectively. The channel is rotated by 45° from the <100> plane. The multi-finger device with 40 parallel fingers, 30 nm of length and 1 µm of width each is designed and embedded in coplanar waveguide access pads for RF characterization. The FDSOI nMOSFET has common source configuration that provides the possibility of 3-port measurement in which the front-gate, drain and the back-gate are referred to RF port1, 2 and 3 respectively. Fig. 1 (left) illustrates the simplified cross section: the device layout features a particular access to the back-gate, including a heavily doped n-type GP located below the BOX and an n-well which provides a natural substrate insulation between the devices (so called flip-well architecture [8]). The schematic of the fabricated double-gate nMOSFET is shown in Fig.1 (right).

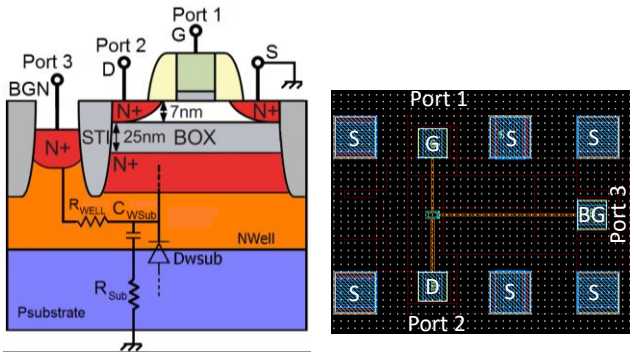

Figure 1. (Left) Simplified cross section and (Right) schematic of studied nMOSFET with back-gate scheme.

"Open" and "short" de-embedding structures are implemented thus allowing for withdrawal of the effects of interconnections on extrinsic capacitances and series resistances. A 4-port Agilent PNAX VNA accompanied with a DC semiconductor-parameter analyzer (HP 4145) are applied to perform the on-wafer 3-port S-parameters measurement up to 26.5 GHz using ground-signal-ground (GSG) pattern infinity probes.

III. 3-PORT RF FOMS EXTRACTION

MOSFET RF performance is evaluated by two major FoM, i.e. f_T and f_{max}. By definition, f_{max} is the frequency at which the (unilateral) power gain is equal to unity (0 dB) and f_T is the unity current gain frequency at which the short circuit current gain (h_{21}) becomes unity (0 dB). f_T and f_{max} are extracted from the measured S-parameters extrapolating h_{21} and unilateral power gain, U, to 0 dB. Similarly to the methodology reported in [9] for 4-port extraction, in case of 3-port S-parameters measurements where port1, port2 and port3 are defined as the front gate, drain and back gate, respectively, h_{21} and h_{23} are defined as:

$$h_{21} = \frac{Y_{21}Y_{33}-Y_{23}Y_{31}}{Y_{11}Y_{33}-Y_{31}Y_{13}} \qquad h_{23} = \frac{Y_{23}Y_{11}-Y_{21}Y_{13}}{Y_{33}Y_{11}-Y_{13}Y_{31}} \quad (1)$$

from which cut-off frequency for front-gate (f_T) and back-gate (f_{Tbg}) can be directly extracted. The unilateral power gain for front gate (U) and back gate (U_{bg}) are calculated from 3-port Y-parameters as:

$$U = \frac{1}{4}\cdot\frac{|Y_{21}-Y_{12}|^2}{Re(Y_{11})Re(Y_{22})-Re(Y_{21})Re(Y_{12})},$$
$$U_{bg} = \frac{1}{4}\cdot\frac{|Y_{23}-Y_{32}|^2}{Re(Y_{33})Re(Y_{22})-Re(Y_{23})Re(Y_{32})} \quad (2)$$

from which the maximum oscillation frequency for front gate (f_{max}) and back gate (f_{maxbg}) are extracted.

Fig. 2 shows the f_T and f_{max} related to the front-gate as a function of V_{gs} for V_{ds} = 1 V and back-gate biases, V_{bg} = 0, 1.8 and 3.0 V. As can be seen in Fig. 2a and b, at V_{bg} = 0 V, the maximum f_T and f_{max} for 30 nm-long device is as high as ~355 GHz. From Fig. 2a and b, it can be seen that application of a positive V_{bg} interestingly shifts the maximum cut-off

frequencies to a lower V_g, however, with slightly decreased peak values. The consequence of the back-gate biasing is firstly, the possibility to get the f_T and f_{max} peak values at lower V_g, as expected, (due to threshold voltage shift with V_{bg}) and secondly, flatter f_T and f_{max} versus V_g curves, i.e. wider V_g range with maximum values of f_T and f_{max}. Fig. 2a includes results for V_d = 0.6 V. One can see that even at such a low V_d, the device features rather high f_T ~280 GHz in a maximum, which is, moreover, stable w.r.t. V_{bg} (inset in Fig. 2a). Considering low voltage and power applications (< 0.6 V), one can get f_T of 280 GHz at V_d =0.6 V as high as f_T for V_d=1V by V_{bg} tuning (example is indicated by arrow in Fig. 2a).

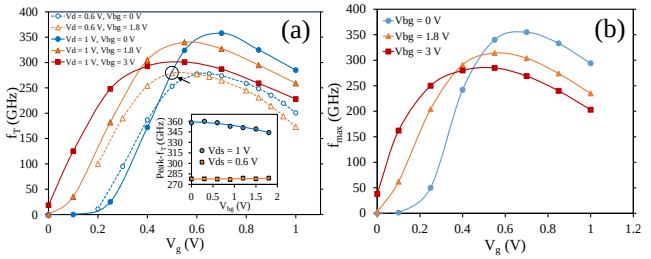

Figure 2. Front-gate (a) f_T for V_{ds} = 0.6 and 1 V and (b) f_{max} for V_{ds} = 1 V as a function of V_g for various V_{bg}.

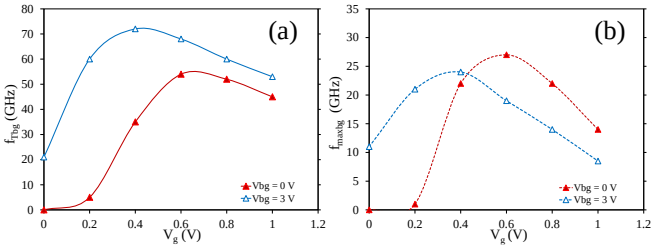

Figure 3. Back-gate (a) f_{Tbg} and (b) f_{maxbg} vs. V_g for V_{bg} = 0 and 3 V.

Plots of RF FoMs related to the back-gate transistor f_{Tbg} and f_{maxbg} are illustrated in Fig. 3a and b versus V_{gs} showing the double gate behavior of FDSOI transistor. From Fig. 3, it can be observed that a maximum f_{Tbg} of 55 GHz – 70 GHz and a maximum f_{maxbg} of 24 GHz – 27 GHz depending on the bias are achieved. The RF FoMs behavior under different V_{bg} is discussed below in terms of small-signal equivalent circuit and parasitic elements.

IV. Model and Extraction

Based on a 3-port model of FDSOI MOSFET shown in Fig. 1, its small-signal equivalent circuit including both intrinsic and extrinsic components is proposed in Fig. 4. By applying different bias conditions, all elements can be extracted (Table I). Clear advantage of 3-port w.r.t. 2-port measurement [4] is the possibility of more complete extraction of parasitic elements such as e.g. well resistance (R_{Well}), total back-gate capacitance (C_{bgtot}), etc.

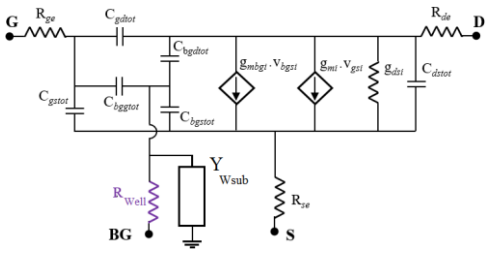

Figure 4. Complete small-signal equivalent circuit of the 3-port FDSOI MOSFET in saturation including the sum of intrinsic ('i') and extrinsic ('e') elements denoted by 'tot'.

Lower g_{mbgi} comparing to g_{mi} (Table I) (due to thicker BOX w.r.t. gate oxide) results, indeed, in a lower f_{Tbg} comparing to f_T (Fig. 2a and 3a) (see Eq.3). As reported in [9], back-gate resistance (R_{bge}), the main reason of f_{maxbg} drop (Eq. 4), is mainly related to the parasitic back-gate network and its value is essentially given by the well. Therefore, f_{maxbg} is much lower than f_{max} (Figs. 2b, 3b) due to 3x higher R_{bg} (R_{Well}) w.r.t R_g (Table I). The reduction of f_T and f_{max} with an increase of V_{bg} for V_d = 1 V case (Fig. 2) can be explained by the g_m (both 'i' and "e") decrease and channel conductance (g_{ds}) increase (Table I). Since f_{max} is dependent on both f_T and g_{ds} (Eq. 4), the degradation effect on f_{max} is more pronounced. As shown in Fig. 3a, an increase of V_{bg} from 0 to 3 V, results in increase of f_{Tbg} which is supposed to be mainly due to C_{bgtot} decrease with V_{bg} increase (Table I). However, f_{maxbg} decreases with V_{bg} increase that could be explained by increasing of g_{ds} dominating over the C_{bgtot} and g_{mbgi} improvement.

TABLE I. Extracted Front- and Back-Gate Elements in Saturation (V_{DS} = 1 V) and Maximum G_{MI} when V_{BG} = 0 V and 3 V.

V_{bg}=3 V			**V_{bg}=0 V**		**Front-gate**			
(mS)	*(mS)*	*(mS)*	*(Ω)*	*(Ω)*	*(mS)*	*(mS)*	*(mS)*	*(fF)*
g_{me}	**g_{mi}**	**g_{ds}**	**R_g**	**R_{sd}**	**g_{mi}**	**g_{me}**	**g_{ds}**	**C_{gtot}**
48	58	7.1	11	5	60.5	50.5	4.5	25.7
V_{bg}=3 V			**V_{bg}=0 V**		**Back-gate**			
(mS)	*(mS)*	*(fF)*	*(fF)*	*(mS)*	*(mS)*	*(Ω)*		
g_{mbge}	**g_{mbgi}**	**C_{bgtot}**	**C_{bgtot}**	**g_{mbgi}**	**g_{mbge}**	**R_{Well}**		
3.7	5	15	21.5	4.8	4.1	30		

$$f_T \approx \frac{g_m}{2\pi C_{gtot}} \quad (3) \qquad f_{max} \approx \frac{f_T}{2.\sqrt{(R_s+R_g)g_{ds}+2\pi f_T R_g C_{gd}}} \quad (4)$$

V. Conclusion

Effect of back-gate bias on RF FoM of front- and back-gate FDSOI MOSFET is studied based on the 3-port measurements. Back-gate bias application shifts and flattens f_T, F_{max} versus V_g curves thus giving more flexibility to the designers for the choice of DC points where maximum f_T and f_{max} is achievable. In low-V_g range (<0.5 V), back-gate bias tuning allows f_T in low-V_d case to outperform f_T in high-V_d case. An equivalent small-signal circuit including back-gate network was reconstructed and main parasitic elements of FDSOI devices were assessed. The effect of back-gate bias on RF FoM was explained through its effect on relevant parasitic small-signal equivalent elements.

Acknowledgment

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Al_2O_3 coating of nanoparticle networks via ALD: effect on strain-sensing performance

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***Abstract*-In the current paper the effect of aluminum oxide coatings (Al_2O_3) fabricated via the Atomic Layer Deposition technique on the stability and sensitivity of nanoparticle based strain sensors is investigated. Thin films of Al_2O_3, varying in thickness, have been deposited on top of a metallic nanoparticle layer. In this way the nanoparticle-strain sensing device is isolated, passivated and protected from environmental factors such as humidity. The level of isolation and the overall effectiveness of the Al_2O_3 depend on film thickness. Optimum Al_2O_3 film thickness is then correlated with short-term device stability and strain sensing sensitivity.**

Nanoparticles; ALD; atomic layer deposition; sputtering; strain sensor; resistance; Aluminum oxide; platinum

I. INTRODUCTION

Metallic or semiconducting nanoparticles have been widely used as materials for sensing applications, for more than 20 years. Our group has been focusing up to now in the use of metallic nanoparticles in particular for chemical, bio and strain sensing applications [1, 2]. In the current paper aluminium oxide (Al_2O_3) coatings are used in tandem with metallic nanoparticle networks, in order to enhance the performance of the device when used as a strain sensor. Al_2O_3 is a well-known dielectric, commonly used as a passivation or protection layer against humidity in microelectronic devices, usually outperforming other materials (e.g. HfO_2) [3]. Here we present results obtained and discuss the influence of Al_2O_3 film thickness in the passivation process of nanoparticle based strain sensors. Interestingly enough we determine that there is an optimum Al_2O_3 thickness where the nanoparticle layer is sufficiently isolated and passivated from the environment; in this case the strain sensitivity of the device is much improved (if compared with uncoated devices) while the short term stability of the sensors is also substantially enhanced.

II. EXPERIMENTAL

Platinum nanoparticles of 5 nm in diameter were produced at room temperature using a magnetron sputtering system. Sputtering allows control over the nanoparticle surface coverage of the substrate, as well as particle size. Nanoparticles were deposited on top of oxidized silicon substrates, previously patterned with gold interdigitated electrodes (IDEs) having an inter finger distance of 5 μm and 10 μm as can be seen in Fig.1.

Following the nanoparticle deposition certain devices have been coated with an Al_2O_3 layer, using the ALD technique. Various thicknesses of Al_2O_3 films (3, 6, 10 and 15 nm) have been used while for all experiments the Al_2O_3 film has been fabricated using a Picosun ALD R-200 reactor. To be more specific, Al_2O_3 ALD was carried out by alternately dosing the following precursors at 80˚C: Trimethylaluminum (TMA, STREM chemicals, 99.99 %) and deionized water. Al_2O_3 film composition has been verified through XPS measurements while film thickness has been estimated using XPS measurements (calculated from the simulation of measured intensity ratios) and ellipsometry.

All strain sensing experiments have been conducted at room temperature using a homemade strain sensing system. The resistance of the devices was monitored in situ using a Keithley 2400 multimeter, as tensile strain was exerted on the sensors.

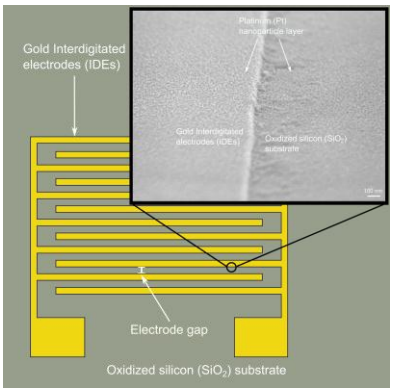

Figure 1. Schematic representation of the gold interdigitated electrodes (IDEs) and SEM image of the platinum nanoparticle layer covering both the SiO2 substrate and the gold IDEs.

III. RESULTS & DISCUSSION

The successful preparation and optimization, in terms of nanoparticle surface coverage, of a nanoparticle-strain

sensor has been previously discussed by this group [1]. The physical explanation behind the increased sensitivity of nanoparticle based devices, when compared to conventional metallic strain gauges or semiconducting strain sensors, lies in the mechanism governing their conductivity. There is an exponential dependence of conductivity with inter-nanoparticle distance, making the sensor extremely sensitive in any respective change. By imposing a tensile strain on the strain sensing devices the inter-nanoparticle distance is increased, leading in turn to an increase of the sensor resistance. The nanoparticle surface coverage plays a critical role in the sensing performance of the device; sensors fabricated having an "intermediate" nanoparticle surface coverage translate in devices just below the so called "percolation threshold". Such devices are on the verge of transcending from an insulating to a metallic conductivity regime, and present increased sensing performance.

Recent publications have stressed the importance of a passivation layer for strain sensing devices [4]. In fact physisorbed humidity on the surface of the sensors has been found to increase the mean inter-nanoparticle distance, thus increasing the resistance of the device and its sensitivity. This phenomenon is further enhanced if tensile strain is applied on the device; this creates more sites for the water molecules to be adsorbed, increasing the swelling of the NP assembly. It is then clear that variations in relative humidity (RH) will affect device resistance and sensitivity. For this reason Al_2O_3 films of varying thickness have been used as humidity-passivation layers. In Fig. 2 the advantages offered with increasing Al_2O_3 film thickness, in the short term stability of the sensors can be seen. Experimental observations after in situ device-resistance measurements, such as drift and thermal noise have been also eradicated with increasing Al_2O_3 thickness. Devices coated with 15 nm of Al_2O_3 have been found to have similar performance with the ones coated with 10 nm and are not included in Fig. 2. Short-term stability of strain sensing devices is of the outmost importance in order to produce a sensitive and reliable device.

The sensitivity of the strain sensing devices (gauge factor) has been calculated before and after the deposition of the Al_2O_3 films. In Fig. 3 can be easily seen the percentile increase in the gauge factor (G) of the strain sensors after the depositon of Al_2O_3 films with varying thickness. For the results shown in Fig. 3, 10 distinctive sensors have been used for each Al_2O_3 thickness. It is interesting to note that by gradually increasing Al_2O_3 film thickness, the gauge factor of the devices also increases up to an Al_2O_3 film thickness of 10 nm (Fig. 3). For Al_2O_3 films having a thickness that was greater than 10 nm, the increase in the gauge factor of the devices is similar to the ones obtained for 3 and 6 nm of Al_2O_3. This phenomenon is currently under investigation by our group and is attributed to the mechanical properties of the Al_2O_3 film and the mismatch between the substrate/platinum nanoparticles layer and the oxide film.

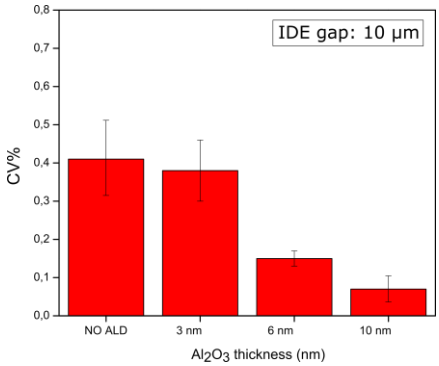

Figure 2. Short-term resistance stability of 10 distinctive strain sensors for each Al_2O_3 thickness, over a period of 30 min. Resistance stability is expressed through the percentage coefficient of variation (CV), also known as relative standard deviation (RSD), The smaller the value of CV the smaller the variability of resistance

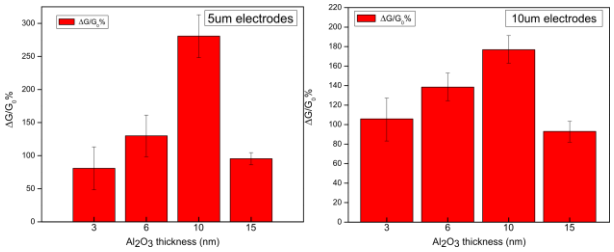

Figure 3. Increase in strain sensitivity/gauge factor (G) in terms of percentile increase, for varying Al_2O_3 thicknesses. The gauge factor for uncoated strain sensors had a mean value of 40.

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Toward the integration of Si nanonets into FETs

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***Abstract*— This paper reports on the first integration of long channel silicon nanonet into a field effect transistor using standard optical microelectronic methods. The electrical characteristics of these devices constituted by randomly oriented silicon nanowires are also studied. Compatible integration on the back-end of CMOS readout and promising electrical performances open new opportunities for sensing applications.**

Silicon Nanowire; Nanonet; Integration; Field Effet Transistor; Morphological and electrical characterizations

I. INTRODUCTION

Silicon nanowire (SiNW) field effect transistors (FET) are potential candidates for biosensing applications [1]. However, their large scale integration remains an ongoing challenge due to time consuming, complex and costly technology[1]. To overcome this issue, an assembly of randomly oriented nanowires called nanonets [2] can be considered with the aim to facilitate their handling and integration while benefiting from the potential of intrinsic nanowire properties. In such networks, current flows via conducting paths involving NW/NW junctions. Despite silicon oxidation under atmosphere, we recently stabilized the electronic properties of Si nanonet resistors using low thermal annealing (≤400°C) treatment [3], offering a broad range of applications. Here, we first demonstrate the fabrication of Si nanonet field effect transistors using standard optical microelectronic methods. Then, the output and transfer characteristics of these devices are studied as a function of the SiNW density in the network.

II. EXPERIMENTAL DETAILS

A. Silicon nanonet fabrication

Silicon nanowires (SiNWs) were synthesized by the so-called Vapor-Liquid-Solid method [4] using dewetted gold thin film as catalyst. Intrinsic single crystals growing along the [111] direction were fabricated. Then, SiNWs were assembled using the vacuum filtration method: after dispersion by sonication of as-grown SiNWs into deionized water, nanonets were successively elaborated after filtration of 18 mL, 24 mL and 34 mL of SiNW solution through a membrane. To ensure reproducibility, the amount of dispersed SiNWs in solution was monitored using absorption spectroscopy [5], [6]. By filter dissolution, they were transferred onto 200-nm thick silicon nitride over heavily doped silicon substrate.

B. Nanonet FET elaboration

Silicon nanonets were integrated into field effect transistors (FETs) with a bottom gate configuration trough standard optical microelectronic process. In order to isolate devices from each other, Si nanonet patterning was performed using dry etching. 200-µm square contact pads were fabricated with standard optical lithography techniques. Prior to metal deposition, native oxide surrounding SiNWs was removed via hydrofluoric acid treatments. Then, a stack of nickel and gold was evaporated using the e-beam method. Nickel was selected for the direct metal contact with SiNWs since the Ni_XSi_Y silicides formed after annealing produce low Schottky barrier with abrupt SiNW/Ni_XSi_Y interface[7], [8]. Thermal annealing at 400°C was performed to promote the electrical contact for both, the Ni/SiNW interface by silicidation and the SiNW/SiNW junction by sintering [3].

III. CHARACTERIZATION METHODS

Morphological characterizations of Si nanonets and devices were carried out by scanning electron microscope (SEM) using Zeiss Ultra+ Microscope. SEM images were analyzed with ImageJ software. Electrical characterizations were performed using a two-probe Karl Süss station controlled by a HP4155A parameter analyzer in a dark environment and at room temperature.

IV. RESULTS AND DISCUSSION

A. Morphology of FETs

A typical nanonet, elaborated with 24 mL of filtered SiNW solution, is presented in Fig. 1 (a). The average length and diameter of the SiNWs in such nanonet were 7 µm and 40 nm, respectively. The percentage of SiNW covering the surface, reflecting the number of SiNWs [5], [6], was estimated for the different volumes of filtered SiNW solution as illustrated in Fig. 1(b). This percentage was tracked after each processing step in order to control the evolution of nanonet morphology during integration.

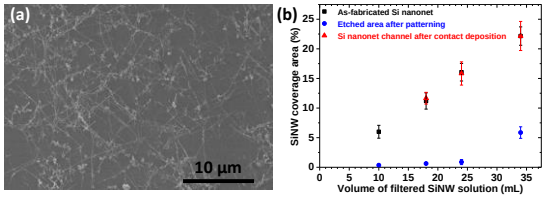

Figure 1: (a) SEM image of typical Si nanonet elaborated with 24 mL of filtered SiNW solution. (b) SiNW coverage area as a function of the volume of filtered SiNW solution after each processing step.

As shown in Fig 1(b), the nanonets were successfully patterned, allowing proper separation between the different devices. Furthermore, the numbers of SiNWs in the FET channel and in the as-fabricated nanonets were matching each other, showing that nanonet morphology was not affected by lithography step.
Figs. 2(a) and (b) display a scheme and an SEM image of the Si nanonet FET, respectively. The Si nanonet channel, highlighted with a red dotted contour Fig. 2(b) is about 50 µm long and 100 µm large.

B. Electrical characteristics

Fig. 3(a) shows typical output characteristics of a 50 µm channel Si nanonet FET elaborated with 34 mL of filtered SiNW solution. The devices displayed p-type operation, with distinguishable linear and saturation regimes in spite of the number of SiNW/SiNW junction (≥8) involved along the conduction paths between source and drain. This proves that Ni/SiNW and SiNW/SiNW electrical contacts were good. The transfer characteristics measured in the linear regime (with -1 V drain voltage) are plotted in Fig. 3(b) for the three volumes of filtered SiNW solution. A saturation current as high as 40 nA was reached at V_g=-25V, along with an ON/OFF ratio larger than 10^3. The increase of the saturation current with the volume of filtered SiNW solution would be consistent with a larger number of conducting paths between source and drain. Electrical performances can therefore be tuned by adjusting the number of SiNWs for the targeted applications.

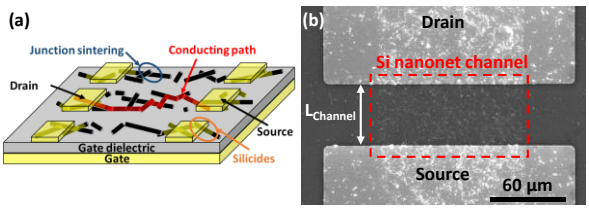

Figure 2: (a) Silicon nanonet-based field effect transistor with a bottom gate configuration. (b) SEM image of Si nanonet FET after processing.

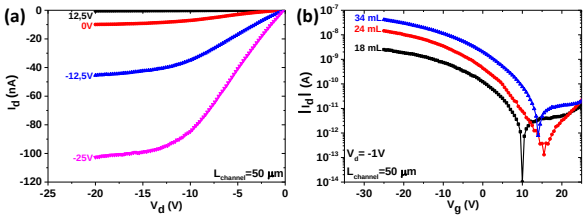

Figure 3: (a) Output characteristics of Si nanonet FET elaborated with 34 mL of filtered SiNW solution. Gate voltages are marked on the curves. (b) Transfer characteristics for different volumes of filtered SiNW solution (drain voltage of -1V). For both (a) and (b), the channel length is 50 µm.

CONCLUSIONS

We have shown the first integration of silicon nanonets into field effect transistors using standard optical microelectronic processes. Good performances were achieved, even with long channels, which involved numerous SiNW/SiNW junctions. Besides, these Si nanonet FETs were fabricated with a low thermal budget (≤400°C), which makes them fully compatible with an integration on top of CMOS back-end. This opens new avenues for the 3D integration of SiNW-based devices such as biosensors.

ACKNOWLEDGMENT

This work has received funding from the EU H2020 RIA project Nanonets2Sense under grant agreement n°688329.

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Si measurements: SiOx on Si

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***Abstract*—We review the results of silicon measurements, which we have performed on sub-oxide SiOx formed on n and p type Si wafers. Localized vibrational modes through Raman and FTIR, light emission properties by photo-luminescence(PL), energy critical points for optical transitions, excited state dynamics and non-linear electrical properties can be used as effective methods in investigating thin oxide layers on Si. Infrared vibrational spectrum of Si–O–Si bondings in terms of transverse-optic (TO) and longitudinal-optic (LO) phonons indicating that disorder induced LO–TO optical mode coupling can be an effective tool in assessing the structural quality of the SiOx. Excited carrier dynamics and switching mechanisms can provide critical information about electronic quality of sub oxides for applications in CMOS circuits.**

Keywords- SiOx on Si, ellipsometry, electrical and optical methods, photoluminescence, FDSOI.

I. INTRODUCTION

SOI technologies such as FD-SOI are very promising cabndidates for future CMOS circuits since they exhibit exciting features for low power and high speed applications. The oxide component forming an important part of this circuitry needs to be evaluated very accurately in terms of electronic quality. This work is devoted to the exploration and evaluation of the main electrical and optical techniques and methodologies to find the most suitable ones in determining the nature of intrinsic and extrinsic properties relating to the performance of MOS device parameters. Finally, the electrical and optical characteristics relating to structural and optical quality will be discussed.

II. TECHNOLOGICAL DETAILS

SiOx on Si layers were fabricated by surface treatment of wafers using HF:HNO3. Thickness, metalization and annealing dependent forming was observed on SiOx cells on Si. Defects and microstructure have been determined by XRD, Raman and FTIR measurements. Room temperature current-voltage characteristics have been carried out using a semiconductor parameter analyser. Time-iresolved and CW PL and ellipsometry measurements were performed at room temperature.

III. RESULTS AND DISCUSSION

PL dynamic relevant to band edge, defects and quantum confinement effects can appear as an effective method of wafer characterization. Ultrafast decay components in the range of ps can be deduced assuming 3-component exponential decay as shown in Fig.1. The ultrafast PL decay leads to a transfer of carriers to long-lived defect states as evidenced by a red emission at around 600 nm. Red shift at initial stages of blue luminescence decay confirms the presence of a possible charge transfer to long lived states. Time-correlated single photon counting measurements revealed life-time of about 5 ns for these states.

Any strain induced defect on SiOx/Si system can result in TO-LO mode coupling of Si-O-Si stretching vibrations at 1100 cm-1, which shifts its position to about 1240 cm-1 at variable angle of incidence of probe beam. This shift can be used to obtain crucial information about the strain/defect induced on any oxide on Si as shown in Fig.2.

Spectroscopic ellipsometry is very effective in determining very accurately energy critical points in SOI system relating to either quantum confinement, defects or high energy band transitions (Fig.3).

Defect induced changes in SiOx and SiOx/Si interface can lead to efficient band edge, quantum confinement and defect related photoluminescence in near infrared as shown in Fig. 4. Room temperature band edge emission with very strong intensity can appear at around 1135-1140nm depending on surface treatment conditions of Si wafer. The sub-gap emission, which appears in some wafers is indicative of point defects.

Figure 5 shows the enlarged I-V curves under positive bias for a closer look of increased current level under the repetitive dc cycling test on SiOx device. A negative differential resistance effect region is shown following the electroforming process in an untreated SiOx device. The data indicates that the current increases linearly with voltage about maximum value, which marks the onset of the reset transition. Above max, the resistance starts to increase, which results in a decrease of current. For larger voltages, the current starts to increase again due to saturation of the resistance.

IV. CONCLUSION

Optical and electrical methods that we presented here can be effectively used in assessing device quality of oxides and thin silicon layers such as FD-SOI. Time-resolved PL for optically active defects and confinement effects, TO-LO mode coupling for strain induced changes, ellipsometry for energy critical points and resistive effects can be suitable methods.

ACKNOWLEDGMENT

This work was supported by THINGS2DO project ENIAC-ECSEL Nanoelectronics under contract≠621221.

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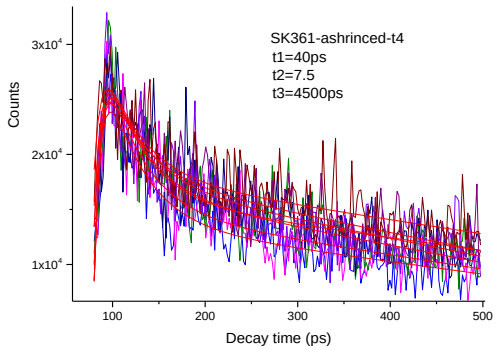

Fig.1 Time-resolved photoluminescence from SiOx layer formed on Si.

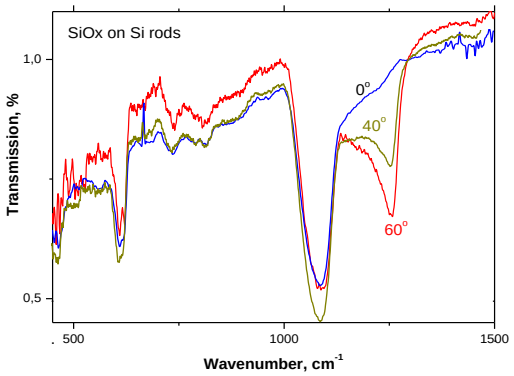

Fig.2 TO-LO mode coupling effect of Si-O-Si. stretching vibrations in SiOx on Si.

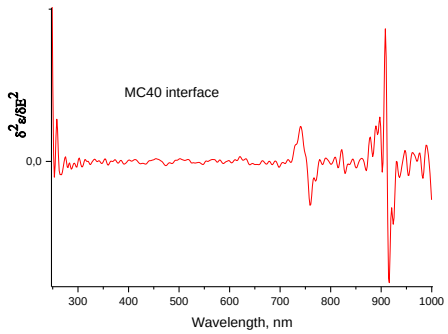

Fig. 3 Energy critical points relating to quantum confinement, defects and E1/E2

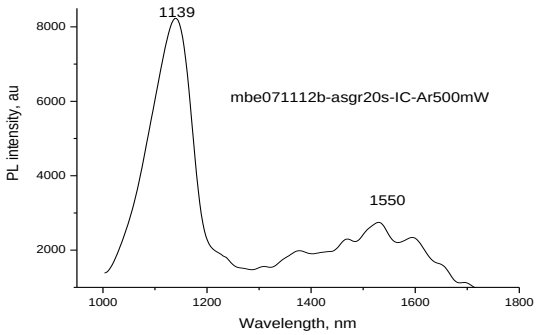

Fig. 4 Room temperature photoluminescence indicating band edge and deep level effects.

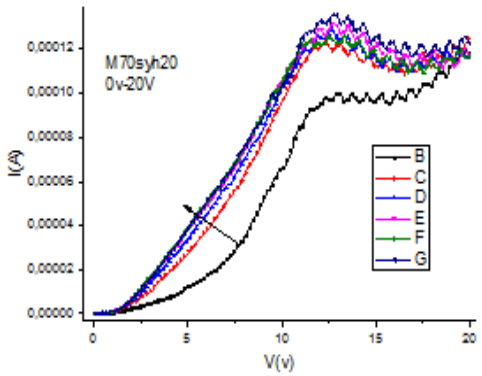

Fig. 5. DC cycling tes**t** in positive polarity on untreated Si/SiOx MOS device

Design and fabrication of a novel power Si/SiC LDMOSFET for high temperature applications

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***Abstract*—In this paper we present for the first time the design and fabrication of a silicon-on-silicon carbide Si/SiC laterally diffused metal-oxide-semiconductor field-effect transistor (LDMOSFET) targeting 200-600 V blocking voltages for high temperature, harsh environment applications such as space and downhole drilling. The final paper will focus on the electrical characterization of this newly fabricated device.**

Keywords-silicon on silcion carbide; SOI; harsh environment; LDMOSFET; power electronics; characterisation; TEM.

I. INTRODUCTION

Electronic devices that are able to work efficiently and reliably at high temperature (300°C and above) are required for harsh environment applications, such as outer space and downhole drilling. Even though SiC devices are emerging with superior electrical and thermal performance, Si and Silicon-on-Insulator (SOI) devices are still dominating the high temperature market. The main reason is that SiC MOS devices have significant channel issues, making them less attractive for medium and low voltage (<1200 V) applications. An alternative solution has been proposed [1, 2], in which devices are fabricated on substrates made from direct wafer bonding of Si and SiC, in which case the high thermal conductivity of the SiC substrate can be utilized to help dissipate the heat generated in the Si active area, minimizing self-heating effects. Previous simulation results demonstrated that with a junction-to-case temperature 4 x less than SOI [3], power transistors with a breakdown voltage up to 600 V are achievable on Si/SiC substrates [4]. In this paper we present for the first time the design and fabrication of a Si/SiC LDMOSFET targeting 200-600 V blocking voltages.

II. EXPERIMENTAL WORK

The 4-inch Si/SiC wafers shown in Figure 1 were prepared by IceMOS Technology Ltd and the bonding process details are published elsewhere [5]. The rippling pattern on the wafer surface is caused by interface strain; trenches (grid pattern in Figure 1) are etched into the Si top layer to partially release it. 1 µm and 2 µm thick n-type Si layers are lightly doped (5-45 Ω.cm) and bonded to the 300 µm thick on-axis semi-insulating ($\geq 1.1\text{x}10^7$ Ω.cm) 4H-SiC substrate. TEM was used to characterize the as-bonded Si/SiC interface. It can be seen that in some areas, such as Figure 2 top, a perfectly homogeneous interface was obtained. In some other places (Figure 2 bottom), features of pits or voids are seen, which may cause charge trapping and Fermi-level pinning there. We previously found out that MOS capacitors fabricated on these as-bonded n-type Si layers showed p-type behaviour and it was suggested that a high density of interfacial charge caused band bending, which in such a thin, lightly doped Si layer inverts the doping polarity of the entire layer [5]. As such, phosphorous was implanted and thermally diffused into the as-bonded Si/SiC wafer surface to obtain an initial Si layer n-type doping of around $2\text{x}10^{15}$ cm^{-3}.

The device structure is shown in Figure 3. Dopants were then ion implanted into selective areas of the device and thermally annealed to form the desired PN junction profiles. Boron was used for P-well ($5\text{x}10^{16}$ cm^{-3}) and P+ region ($5\text{x}10^{19}$ cm^{-3}), phosphorous for N-well ($5\text{x}10^{16}$ cm^{-3}) and arsenic for N+ regions ($1\text{x}10^{20}$ cm^{-3}). After standard RCA 1 and 2 cleaning procedures, 500 nm of SiO_2 was deposited on the sample surface via PECVD to passivate the Si surface dangling bonds. Gate regions were opened via UV photo-lithography and RIE etching of the passivation SiO_2. Gate oxide was grown in 5 L/min O_2 at 900 °C for 6 hours to obtain a thickness around 60 nm, after which a further 1 L/min N2O annealing at the same temperature was applied to densify the gate and surface passivation oxide. 500 nm Al was deposited in the selective areas using an e-beam evaporator to form the gate, source and drain terminals. Finally, the device was annealed in forming gas ($5\%H_2/95\%N_2$) at 450 °C for 2 hours to make Ohmic contacts at source and drain. The forming gas process also helps to reduce MOS interface trap densities.

Characterization of the fabricated device is being carried out and the electrical performance will be presented in the full paper.

III. FIGURES

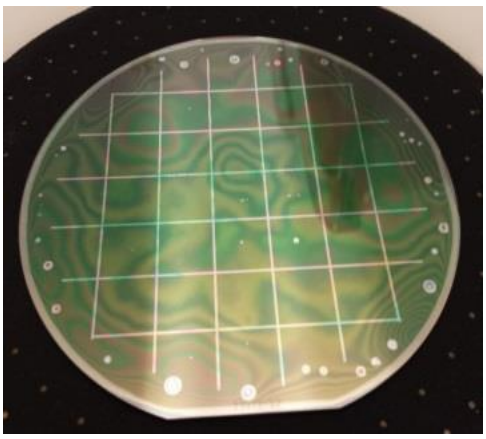

Figure 1. Four inch bonded Si/SiC wafer with 1 µm Si layer

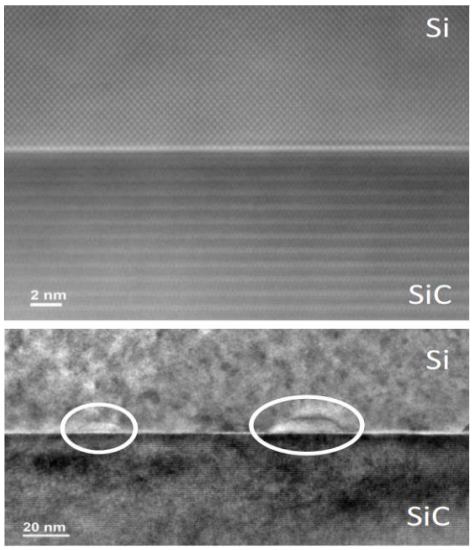

Figure 2. A TEM image of (top) homogeneous, oxide and defect free area and (bottom) another area where voids or pits are present.

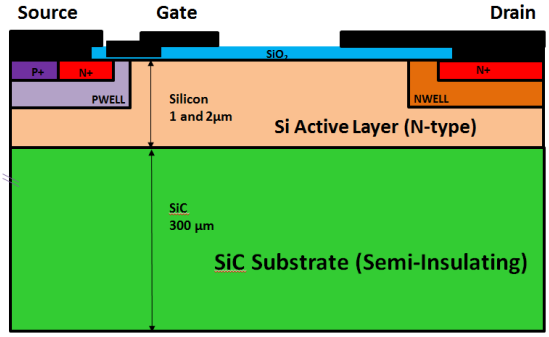

Figure 3. Schematic graph of the fabricated Si/SiC LDMOSFET structure.

ACKNOWLEDGEMENTS

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Gate capacitance performance of p-type InSb and GaSb nanowires

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***Abstract*—The electrostatic behavior of p-type nanowires made of antimonide III-V materials (InSb and GaSb) is analyzed by means of a self-consistent solution of the Poisson and Schrödinger equations, under the k·p approximation. The results are compared to those achieved for Si and Ge NWs, and the contribution of each of the capacitance terms (quantum and inversion layer capacitances) is thoroughly analyzed.**

Keywords- III-V semiconductors, p-type semiconductors, gate capacitance.

I. Objective and Numerical Approach

III-V nanowires (NWs) have attracted extensive research interests in recent years because of their unique physical properties. For the practical implementation of CMOS circuits based on NWs, p-channel FETs are needed. Several materials are currently being investigated as technologically relevant p-type semiconductors. In particular, increasingly more attention has been focused on InSb and GaSb owing to their excellent hole transport properties [1]. In this work we study the electrostatic properties of small NWs made of these materials and carry out a comparison with equivalent devices based on Si and Ge.

While the effective mass approximation (EMA) can be used to describe the Conduction Band (CB) of most semiconductors, this approach fails in the description of the Valence Band (VB) and more complicated models have to be employed to take into account the coupling of the different subbands forming the VB (Heavy Holes, Light Holes and Split-Off). Moreover, the coupling between the VB and the CB has to be considered for direct small-gap materials, such as III-V compounds. Thus, to analyze p-type NWs, we have developed a numerical tool that self-consistently solves the Poisson and the Schrödinger equations, being the VB described by means of an eight-band *k·p* model which accounts for the coupling between the VB and the CB. For indirect group IV semiconductors, a simplified six-band *k·p* model has been used, since the coupling of the CB and the VB is considered as negligible. To accurately reproduce the cylindrical geometry while taking into account crystal anisotropy, the Finite Elements Method has been employed to discretize and solve the resulting equation system [2].

II. Results

In this study we have considered a cylindrical NW with 5nm diameter, oriented along the [111] direction. Four different devices have been simulated, each of them corresponding to the following materials: InSb, GaSb, Si and Ge. In all the cases, the same insulator (Al_2O_3) with a thickness of 1.5nm has been used. This way, identical contribution of the insulator capacitance for all NWs is attained, so that we can focus on the channel material behavior. Fig. 1 shows the bandstructure at a gate overdrive voltage of -0.4V. The energy is referred to the VB edge, and the Fermi level (E_F) is depicted by a dashed grey line. The threshold voltage (V_T) is calculated from the maximum of the second derivative of the charge with respect to the gate voltage [3]. A quite different scenario is observed between Si and the other three channel materials. The former shows a large number of bands per unit energy with a lower curvature, which corresponds to a higher DOS and higher effective mass as compared to the latter. Fig. 2 presents the gate capacitance behavior as a function of the gate overdrive voltage. As shown, despite the noticeable differences found in the band structure of each of the studied NWs, the performance in terms of the C_G is quite similar for all of them. To analyze this effect, we have separated and depicted the three terms determining the gate capacitance: quantum capacitance (C_q), centroid capacitance (C_C) and insulator capacitance (C_{ins}) [4]. C_q behaves as expected from the DoS of each material, with the largest value achieved by the Si NW, and the lowest by the InSb one. As for the C_C term, it is strongly related to i) the dielectric constant of the semiconductor, and ii) the charge centroid position. As the dielectric constant of Si is lower than the one of the other materials, a lower C_C in the subthreshold regime is achieved for Si, as the charge is basically placed at the same position regardless the employed material. This can be checked by depicting the charge centroid position (Fig. 3), which has been calculated as in [4]. As the gate overdrive voltage is

increased, the centroid of III-V NWs and Ge becomes larger than the calculated for Si devices. This fact produces a compensation of the higher values of their dielectric constant, and, as a consequence, the C_G values for the four considered devices become very similar.

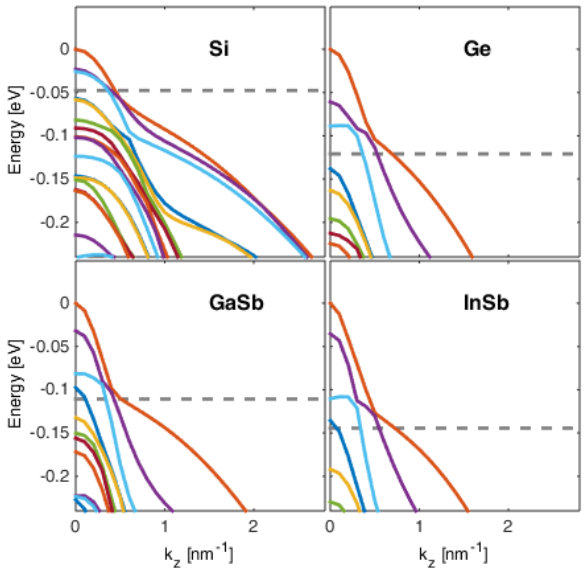

Figure 1. Band structure achieved at V_G-V_T=-0.4V for the four devices under study. The energy is referred to the maximum value of the VB, while the Fermi energy is depicted as a horizontal dashed line.

III. Conclusion

A numerical simulator that self-consistently solves the Poisson equation and the eight-band *k·p* method in the cross section of 5nm cylindrical NWs has been developed. A comprehensive study of the electrostatic performance of this device has been carried out focusing on p-type channels and four different materials: Si, Ge, InSb and GaSb. Our results indicate that, in spite of their low effective mass and small density of states, GaSb and InSb NWs hold the comparison with Si and Ge in terms of gate capacitance and inversion charge. The good electrostatic performance, combined with the expectation of excellent transport characteristics, place GaSb and InSb as attractive alternatives for p-type devices on CMOS logic based on NWs.

Acknowledgment

This work was supported by the Spanish Government under the Project TEC2014-59730-R. C. Martínez-Blanque acknowledges the Junta de Andalucía support under project P09-TIC4873. A. Toral also acknowledges the University of Granada funding through the Becas de Iniciación a la Investigación para alumnos de Máster. J. M. González-Medina also acknowledges grant FPU014/02579.

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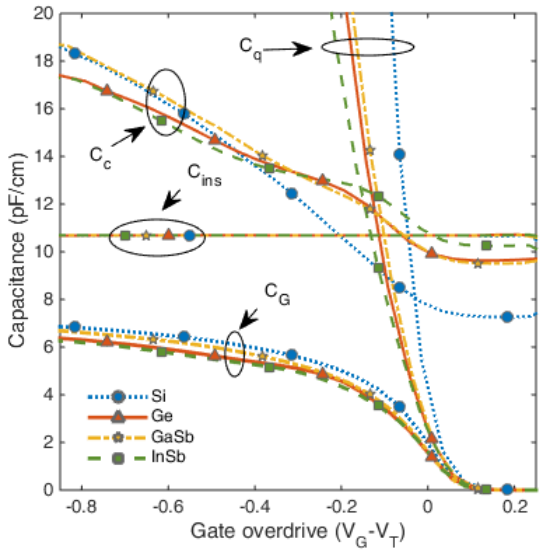

Figure 2. Gate capacitance (C_G) as a function of the gate overdrive voltage (V_G-V_T). C_G can be calculated as the series combination of the three other terms depicted: C_{ins}, C_c and C_q.

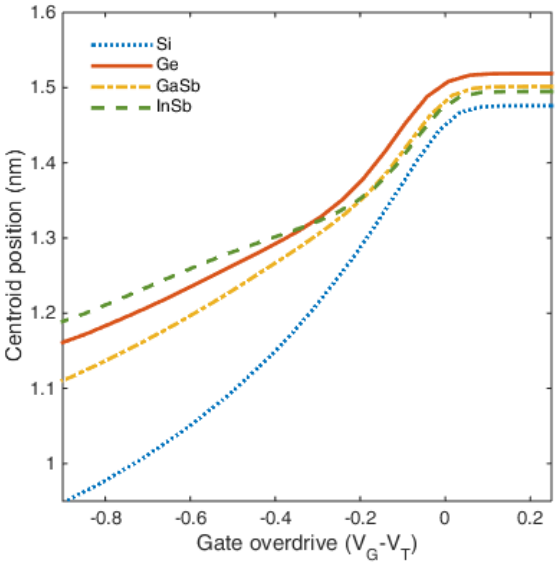

Figure 3. Charge centroid position as a function of V_G-V_T for each of the devices under study. The centroid is referred to the semiconductor/insulator interface, i.e., a larger centroid implies a higher separation of the charge from the insulator.