Transistor architecture and channel materials for nanoscale FET

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Abstract

Driven by the needs of traditional area scaling transistor architecture has evolved significantly in the last few CMOS technology nodes, with an evolution towards 3D transistor architectures such as finFET devices. Further scaling requires besides area reduction, power and performance improvements, which can be provided through a close interaction between design and technology.

In this talk we will explore a few CMOS scaling pathways, with a focus on the interaction between design choices and transistor architecture. We will explore the transition from finFETs to gate-all-around (GAA) devices at advanced nodes, and the advantages of each choice. We will also have a look at the impact and challenges of introducing high mobility materials, such as Ge and III-V channels.

Modeling and Design Considerations for Negative Capacitance Field-Effect Transistors

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***Abstract*—Stabilization of ferroelectric negative capacitance (NC) in a transistor gate stack is a promising pathway towards future low power electronics. However, most modeling efforts of such NCFETs are based on single-domain Landau theory, which is an oversimplification that leads to incorrect predictions and device design. By extending the Landau model to describe more than one domain, it is shown how an internal metal electrode inherently destabilizes NC. Consequently, NCFETs have to be designed without internal metal electrode to function. Furthermore, the use of single-domain Landau theory to model NCFETs with HfO_2 based ferroelectrics is critically discussed.**

Keywords-negative capacitance; ferroelectric; domains

I. Introduction

In order to reduce the power consumption of highly integrated circuits, the supply voltage has to be decreased without compromising device performance. To achieve this goal, the use of ferroelectric (FE) negative capacitance (NC) to lower the subthreshold swing of a field-effect transistor (FET) below the thermionic limit of $\ln(10)k_BT/q$ was proposed [1]. While there are already several experimental confirmations of the NC effect [2-5], so far most of the modeling efforts have focused on single-domain Landau theory to describe the FE instability. Especially, the use of an internal metal electrode between the FE and the gate dielectric has been proposed, not only because it is easier to simulate, but also as a solution to mitigate polarization non-uniformity of the FE [6-10]. However, it will be shown that an internal metal electrode will inherently destabilize NC, making it undesirable for steep slope devices. Furthermore, the applicability and limitations of single-domain Landau theory to model NCFETs using HfO_2 based FE materials will be discussed.

II. Multi-Domain Landau Modeling

For clarity, we employ a FE model with exactly two domains and use a linear capacitor for the FET gate capacitance in series as shown in **Fig. 1**. Each domain is modeled as a separate FE capacitor with charges Q_1 and Q_2 in parallel. Leakage, which can also destabilize NC with an internal metal electrode, is neglected here [11]. The free energy of each domain $U_{1,2}$ is described by a Landau expansion of the corresponding charge $Q_{1,2}$.

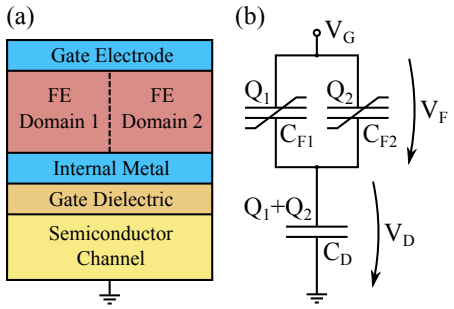

Figure 1. (a) Schematic gate stack of an NCFET with internal metal. (b) Equivalent circuit used for multi-domain simulations.

$$U_{1,2} = \alpha Q_{1,2}^2 + \beta Q_{1,2}^4 - V_F Q_{1,2} \quad (1)$$

Here, α and β are the anisotropy constants of the FE and V_F is the voltage across the FE. Using $\alpha = -6.7\text{x}10^9$ V/C and $\beta = 1.8\text{x}10^{28}$ V/C^3 the free energy of the FE ($U_F = U_1 + U_2$) as a function of Q_1 and Q_2 is calculated and shown in **Fig. 2** (for $V_F = 0$). It is apparent that there are four degenerate energy minima in the corners of the contour plot corresponding to: Both domains switched up (↑↑), both domains switched down (↓↓), domain one up and domain two down (↑↓), and domain one down and domain two up (↓↑). The energy maximum at Q_1=Q_2=0 coincides with the NC region, since capacitance can be defined as one over the second derivative of the free energy with respect to the charge [3]. To stabilize this NC region it was proposed to connect a dielectric capacitor in series to the FE [1]. The free energy of this capacitor C_D is then given by

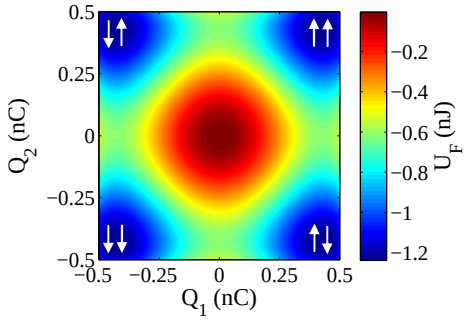

Figure 2. Free energy of the ferroelectric U_F as a function of domain charges Q_1 and Q_2. Arrows indicate polarization directions.

$$U_D = (Q_1 + Q_2)^2/(2C_D) - V_D(Q_1 + Q_2), \qquad (2)$$

where V_D is the voltage across C_D, see Fig. 1(b). Similarly to Fig. 2, U_D can now be plotted as a function of Q_1 and Q_2 as shown in **Fig. 3** (for V_D = 0, C_D = 100 pF). Since U_D is a quadratic function of the total charge Q_1+Q_2, the energy landscape describes a parabola along the Q_1=Q_2 diagonal (single domain case), which extends along the Q_1=-Q_2 axis where the total charge is constant. With Eq. (1) and (2), the total energy of the system can be calculated as $U_T = U_F + U_D$, as shown in **Fig. 4** (for V_G = 0). As can be seen, the series connection of C_D only eliminates two of the four FE energy minima (↑↑ and ↓↓) through the depolarization energy of the dielectric. However, the minima corresponding to oppositely switched domains (↑↓ and ↓↑) prevail. While for Q_1=Q_2 the NC regime is stabilized, even the smallest perturbation which results in $Q_1 \neq Q_2$ leads to spinodal decomposition into a multi-domain state. Consequently, in any multi-domain FE, NC cannot be stabilized with an internal metal electrode, since each FE domain has to be stabilized individually.

III. Implications for HfO_2 based NCFETs

The most promising materials for NCFETs are HfO_2 based FEs, because of their high scalability and Si process compatibility. However, the common use of single-domain Landau theory to fit α and β from the polarization-voltage hysteresis of HfO_2 based FE capacitors is highly questionable [8-10,12]: Firstly, HfO_2 based FEs are polycrystalline materials [5,13], which also contain non-FE grains, especially at film thicknesses of 5 nm and below. Therefore, the "real" P_r might be very different from the extracted one, if e.g. only 10% of the film is FE [8,12]. Secondly, non-uniformity of the FE has to be incorporated into the model, since no internal metal electrode can be used and therefore, distributions of grain size and orientation will strongly influence the device behavior [5,13]. So far, no NCFET simulation has considered these critical effects.

IV. Conclusions

By applying Landau theory, we have shown that the use of an internal metal electrode between a FE and a dielectric will inherently destabilize NC due to domain formation. Therefore, NCFETs have to be designed without internal metal electrode to work as steep slope devices. Furthermore, HfO_2 based FEs are most promising for NCFETs, but models have to consider the grain and domain structure of the material to correctly estimate anisotropy constants and model NCFET devices.

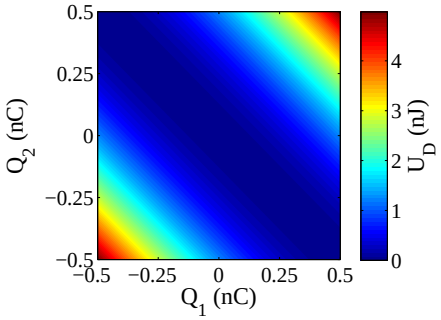

Figure 3. Free energy of the dielectric capacitor U_D as a function of the domain charges Q_1 and Q_2.

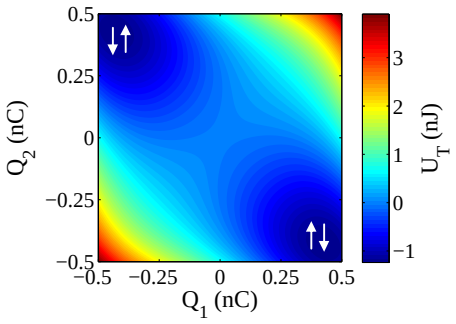

Figure 4. Total free energy U_T of the ferroelectric-dielectric system as a function of the domain charges Q_1 and Q_2. Arrows indicate polarization directions.

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On quantum effects and Low Frequency Noise spectroscopy in Si Gate-All-Around Nanowire MOSFETs at cryogenic temperatures

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***Abstract*— In this work, DC and low frequency noise have been investigated in Gate-All-Around Nanowire MOSFETs at very low temperatures. Static characteristics at 4.2 K exhibit step-like effects that can be associated to energy subbands scattering while the low frequency noise spectroscopy (from 10 K to 70 K) leads to the identification of Silicon film traps.**

Gate-All-Around; SOI MOSFET; nanowire; cryogenic temperature; low frequency noise; noise spectroscopy

I. INTRODUCTION

Gate-All-Around (GAA) nanowire MOSFETs are known to be promising according to the International Technology Roadmap for Semiconductors in order to reach the sub-10 nm technology specifications [1]. Very low temperatures allow electronic devices to reach improved performances as a comparison to room temperature, but can lead to changes in the electronic transport mechanisms. Moreover the space industry often uses cryogenic temperatures in their applications [2].

This paper details the studies carried out at very low temperatures for an imec n-channel GAA NW MOSFET. The gate length is L_G = 45 nm, the width is W_G = 425 nm (5 nanowires of 20 nm width and 22-23 nm height). The equivalent oxide thickness is EOT = 1.9 nm and the surface gate oxide capacitance is $C_{ox} = 1.79 \cdot 10^{-6}$ F·cm^{-2}. Full device details can be found in [3]. Static and Low Frequency Noise (LFN) measurements have been performed in the linear operation regime, with liquid Helium and the help of a Lakeshore TTP4 probe station and a Lakeshore 331 Temperature Controller. Further detailed analysis will include impact of the channel length for n and p-channel GAA NW MOSFETs and comparisons with FinFETs and also the impact of the subband scattering effect on the low frequency noise.

II. STATIC PERFORMANCES AT 4.2 K

Typical conductance characteristics $G_{DS}(V_{GS})$ in the linear operation regime can be found in Fig. 1. The transistor conductance G_{DS} is supposed to be independent of the drain voltage V_{DS}, however G_{DS} characteristics do not superpose for $V_{DS} \leq 1$ mV but they do for higher drain voltage values. This phenomenon might be explained by subband scattering, i.e. the fact that the conduction band is split in discrete subbands at very low temperature. However this can be observed only if the contribution $q \cdot V_{DS}$ (q is the electron charge) of the drain voltage and $k_B \cdot T$ (k_B is the Boltzmann constant) of the thermal energy are not much higher than the energy spacing between the subbands ΔE [4].

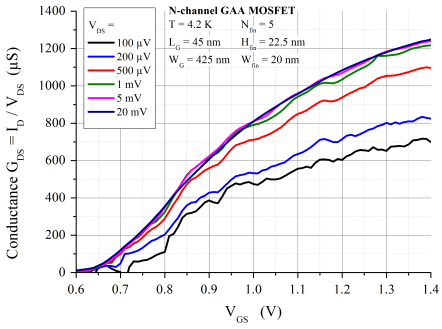

Figure 1. Typical conductance characteristics $G_{DS}(V_{GS})$ in linear operation regime.

The transconductance characteristics g_m normalized by the drain voltage are shown in Fig. 2. Characteristics at low V_{DS} exhibit several valleys with local minima (numbered from 1 to 8). These might be attributed to the successive filling of the energy subbands by increasing V_{GS}, causing the drain current I_D to have a step-like evolution. The gate voltage spacing ΔV_{GS} between these minima can lead to the experimental subband energy spacing $\Delta E = \Delta V_{GS} (\pi \hbar^2 C_{ox}) / (2 m^* q)$, where ħ is the reduced Planck constant, m^* is the electron effective mass ($0.19 \times 9.1 \cdot 10^{-31}$ kg) [5]. From the values in Fig. 2 one can estimate the subband energy spacing in the range 2 meV to 6 meV, which validates our assumption that $q \cdot V_{DS} < 0.5$ meV (for $V_{DS} < 500$ µV) and $k_B \cdot T$ = 0.362 meV are small enough compared to ΔE in order to observe subband scattering. Furthermore one can notice that the transconductance for V_{DS} = 20 mV shows significantly less oscillations, as expected. This is due to $q \cdot V_{DS}$ that is now significantly larger than ΔE, implying that many of the first subbands are already populated.

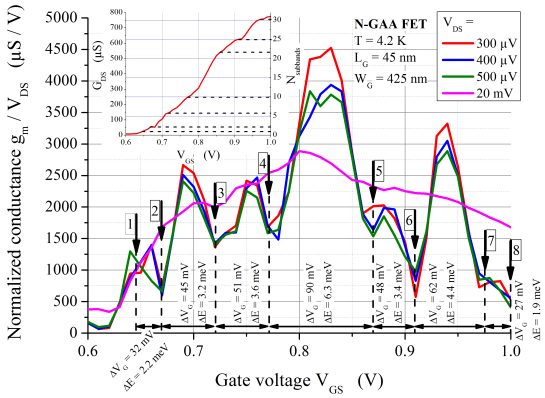

Figure 2. Transconductance $g_m(V_{GS}) / V_{DS}$ of an N-channel GAA MOSFET showing the slope discontinuities at low drain voltage V_{DS}. Arrows show the local minima linked to the subbands. Inset: conductance at V_{DS} = 300 µV and corresponding number of subbands.

The step-like effects can also be seen with the conductance G_{DS} in the inset of Fig. 2. We can see on the Y-right axis that the height of the first step is the same as the spacing between the first and the second. Thus this may correspond to the filling of a single subband. However the spacing between the other steps seems to be multiples of the first one, leading to the assumption that several subbands are populated at once [5].

III. Low Frequency Noise Spectroscopy

Low Frequency Noise spectroscopy can be used as a non-destructive diagnostic tool in order to identify Silicon film traps and estimate their density. First the gate voltage noise Power Spectral Densities (PSD) Sv_g are measured as a function of V_{GS} and the temperature. A model is used taking into account the white noise (of level K_w), the 1/*f* noise (level K_f) and the Generation-Recombination (GR) noise contributions (Lorentzians of plateau level A_i and characteristic frequency $f_{0,i}$) [6] as seen in the inset of Fig. 3. From the extracted parameters, one can study the evolution of $f_{0,i}$ as a function of the gate voltage. Only characteristic frequencies that are independent of V_{GS} and which may be attributed to defects in the silicon film are taken into account [7].

For those Lorentzians, the Arrhenius diagram can be plotted as on Fig. 4. Linear regressions lead to the identification of the traps by comparing values of ΔE (difference between the conduction band energy level E_C and the trap energy level E_T) and σ_n (trap capture cross-section) to literature data, according to the formula in Fig. 4. [8].

Although few points are used, we have identified two traps. The first trap, denoted D1, can be associated to C_iC_s (0/+) and the second one, D2 is unknown. However, the nature of these traps is similar to results that have been obtained using LFN spectroscopy for FinFETs made with the same technology [9] (same ΔE, σ_n in the same order of magnitude and same temperature range where traps are active).

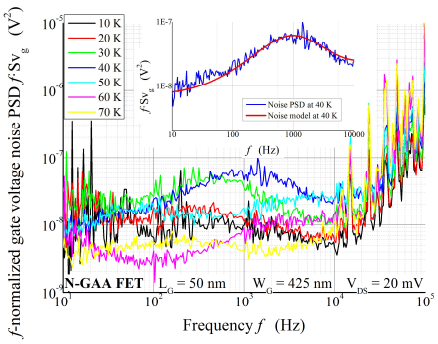

Figure 3. Gate voltage noise PSD Sv_g as a function of the temperature. Inset: noise model at 40 K using $Sv_g = K_w + K_f / f + \sum [A_i / (1+(f/f_{0,i})^2)]$

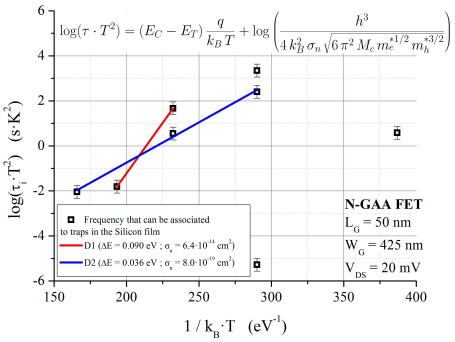

Figure 4. Arrhenius diagram leading to identification of Si film traps.

IV. Conclusion

Static characteristics at 4.2 K show step-like behavior that is most likely due to subband scattering. The low drain voltage (when V_{DS} < 500 µV) and the low temperature (4.2 K) are sufficiently low to highlight the quantum impact of the energy subband scattering. LFN spectroscopy allows identifying silicon film traps. Two defects have been found in the studied GAA and they are of the same nature as in the same technology FinFETs. Further discussions will be done about the evolution of the subband scattering effects and low frequency noise as a function of the temperature (4.2 K to 70 K) in different geometries of n and p-channel GAA MOSFETs.

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First SOI Tunnel FETs with Low-Temperature Process

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1. Abstract

We demonstrate for the first time the fabrication and electrical characterization of planar SOI Tunnel FETs (TFETs) with low temperature (LT) processes devoted to 3D sequential integration. The electrical behavior of these TFETs, with junctions obtained by Solid Phase Epitaxy Regrowth, is analyzed and compared to reference samples (regular process at high temperature, HT). The threshold voltage (V_{TH}) of p-mode operating TFETs shows a 300 mV reduction with similar ON state currents (wrt HT ref.), opening path towards optimized devices (very low V_{TH} & supply voltage V_{DD}).

Keywords: Tunnel FET, TFET, low temperature, SPER, tunneling, BTBT, Coolcube, 3D sequential integration

2. Introduction

TFETs (Tunnel FETs) are p-i-n gated diodes (Fig.1) yielding extremely low OFF currents and, in theory, lower subthreshold swing (SS) below the CMOS 2.3·kT/q limit [1]–[5]. These properties make TFETs very attractive for ultra-low power applications (V_{DD}<0.5V). TFETs exhibit significant differences compared to regular CMOS devices: i) The ON state current is ruled by the band-to-band tunneling (BTBT) carrier injection, ii) a single TFET device can be used either in p- or n-operation modes. Up to now, we have fabricated TFETs with regular CMOS process flow (*i.e.*, with high temperature recipes for gate stack, spacers, epi and junctions). Recently low temperature processes have been demonstrated to be suitable for 3D sequential (CoolCube™) integration [6]. In this work, we investigate for the first time **Tunnel FETs fabricated with low temperature (LT) processes**, showing their **compatibility with 3D sequential architectures**. These LT devices are also compared to regular high temperature (HT) TFETs. Besides **electrical measurements**, **TCAD simulations** have been performed to investigate the junction-related electrical differences.

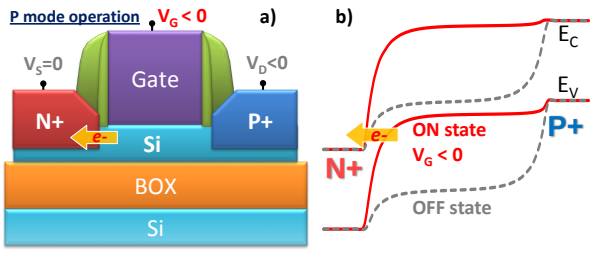

Fig. 1: *a)* TFET bias scheme for p-mode operation; *b)* Corresponding band diagrams illustrating the OFF and ON states.

3. Low-Temperature TFET Process

We have fabricated MOSFETs and TFETs on 300 mm SOI wafers (11 nm thick Si starting film) with the process flow (described in Fig. 2), featuring PolySi/TiN/HfO_2 gate stack. Then the first spacers have been formed at low temperature (630°C). Intrinsic $Si_{0.73}Ge_{0.27}$ selective epitaxy was used to thicken the raised sources and drains regions epitaxy (at T=630°C) was used instead of Si RSD (at T=750°C). In our extension last (Xlast) integration scheme [6] for LT devices, junctions are implanted after RSD epitaxy. Dopants activation is achieved thanks to i) SPER at 600°C for 2 min with modified implantation conditions (LT process) or ii) a 1050°C spike anneal after standard LDD+HDD implantation (HT process). The Back End process ends with the Metal 2 module.

High Temperature (HT) *1050 °C max.*	Low temperature (LT) *630 °C max.*
SOI : Si 11 nm / 145 nm BOX)	
Si MESA patterning	
Gate stack deposition, litho., etching PolySi 50 nm / TiN 6.5 nm / HfO_2 (525°C)	
Spacers 1 (nitride)	
$Si_{0.73}Ge_{0.27}$ Raised Source-Drain epitaxy (630°C)	
LDDp (extensions p) lithography	
BF2 implant	Ge Pre-amorphization implant (PAI) *see TEM image in Fig. 3* + B implant
LDDp (extensions p) resist stripping	
LDDn (extensions n) lithography	
As implant	Ge Pre-amorphization implant (PAI) + P implant
LDDn (extensions n) resist stripping	
Anneal **950°C** Spike	Anneal **600°C** 2 min (**SPER**)
Spacers 2 (nitride / oxide)	
HDDp (litho., B & BF_2 implants, strip)	
HDDn (litho., As & P implants, strip)	
Dopant activation **1050°C** spike	
NiPt silididation, Back-end process	

Fig. 2: Simplified process flow for CMOS, TFET fabrication. The new low temperature process with Xlast and SPER techniques (LT: 630°C) is compared to the standard (HT: 1050°C) process.

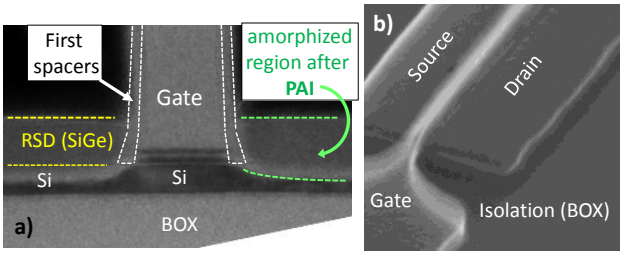

Fig. 3: *a)* Cross-sectional TEM picture of a LT device after Pre-amorphization implant (PAI), showing the amorphized region prior to dopants implantations; *b)* tilted SEM picture of a MOSFET after extension (LDD) formations.

4. Electrical Characterization

We have investigated the impact of the LT and HT processes on the electrical characteristics of TFETs working in p-type operation mode. We first have verified the TFET behavior of the fabricated devices with the swapped dual I_D-V_{DS} technique [7] (and the good CMOS behavior: not shown here): Fig. 4 shows that the devices used in this study are real TFETs and not Schottky based transistors.

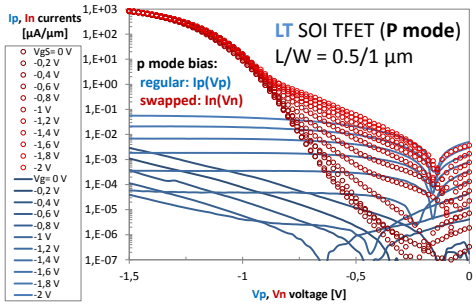

Fig. 4: Example of dual $I_D(V_{DS})$ measurements performed on the fabricated devices (according to the TFET validation method detailed in [7]) showing that tunneling is BTBT and not Schottky related.

The electrical performance in Fig. 5 shows a very low dispersion of the I_D-V_G curves within a given wafer. This small variability indicates that both HT and LT processes are well controlled. Moreover the use of the LT process leads to a V_{TH} reduction (~ 300mV) and to a degraded leakage (I_{OFF}), which could be attributed to the SPER related defects not entirely healed in this thick Si film. This results for $I_{ON}(I_{OFF})$ plots (Fig. 6) in a promising increase of the I_{ON} current for LT of ~100-200% with respect to the HT one.

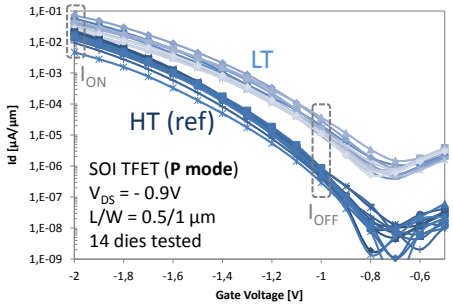

Fig. 5: Measured p-mode $I_D(V_{GS})$ of SOI Tunnel FETs fabricated with high-temperature and low-temperature processes.

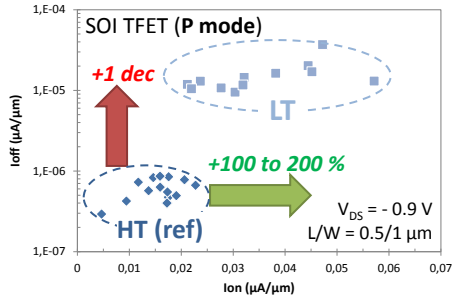

Fig. 6: Impact of TFET process (HT vs. LT) on $I_{ON}(I_{OFF})$ plots with I_{ON} at V_{GS} = -2V & I_{OFF} at V_{GS} = -1V (for p-mode TFETs).

The subthreshold swing extractions in Fig. 7 show very similar performance. As the process is not optimized for tunneling switches, the minimum slope (160 mV/dec) remains above the theoretical 60 mV/dec value.

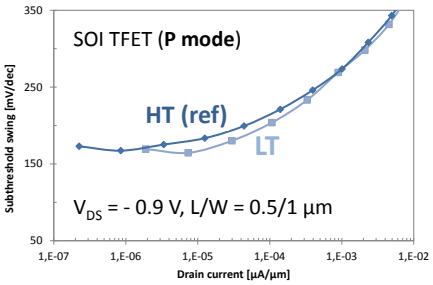

Fig. 7: Figure of merit SS(I_D) of p-mode TFETs (for HT vs. LT devices) at V_{DS} = -0.9 V.

2D TCAD simulations (with full silicon Source, Drain and channel) were conducted to analyze the physical reason for the measured HT/LT differences. We assumed dopant profiles parameters (lateral junctions position, abruptness) typical of the HT and LT processes: overlapped junctions with standard abruptness for HT and underlapped abrupt junctions for LT. Even if this description does not exactly correspond to the real doped regions, it enables to catch the difference in terms of tunneling efficiency. I_{ON} is here defined at a given gate overdrive (V_{GS}-V_{TH}) in order to get rid of V_{TH} difference (Fig. 8). One can note that HT structures yields the best measured relative Ion performance although the LT one is close.

I_{ON} at V_{GS}-V_{th}=-0.7 V		HT (ref.) TFET	LT TFET
Measured Ion		~17 nA/µm	**~10 nA/µm**
TCAD	*Ion*	*~3.3 nA/µm*	***~0.87 nA/µm***
	Junction position	*+7 nm (overlapped)*	*-4 nm (underlapped)*
	Abruptness	*1.5-2 nm/dec (II+anneal)*	*0.5-0.7 nm/dec (SPER)*

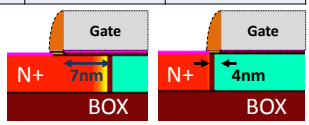

Fig. 8: Tentative comparison of HT/LT performance by TCAD simulations and measurements. Relative I_{ON} (at V_{DS} = -0.9 V) comparison between electrical measures & TCAD simulations for HT/LT dopant profiles assumptions.

6. Conclusion

This work demonstrates the successful integration of low-temperature (630°C) TFETs and their electrical analysis (measurements, TCAD). We observe the same low variability as for reference (1050°C) devices and point out the impact of the junction on the performance. These new results i) provide optimization paths for low V_{DD} operating planar Tunnel FETs, ii) and show the TFET potential for 3D sequential integration.

Acknowledgement

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Impact of strain and traps on optimized n- and p-type TFETs

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***Abstract*— A simulation study on the impact of interface traps (ITs) and strain on the I/V characteristics of co-optimized n- and p-type tunnel field-effect transistors (TFETs) realized on the same InAs/$Al_{0.05}Ga_{0.95}As$ technology platform is carried out using a full-quantum simulator. In order to capture the effect of interface/border traps on the device electrostatics in a way consistent with the ballistic approach, the classical Shockley-Read-Hall theory has been properly generalized. Traps induce a significant reduction on the ON-current. The inclusion of a uniform strain induces a remarkable current enhancement able to completely recover the current degradation.**

Keywords- Tunnel Field-Effect Transistors (TFET), III-V materials, strain, interface traps, quantum transport

I. INTRODUCTION

Tunnel FETs (TFETs) are considered one of the most promising alternatives to the conventional CMOS technology in the quest for the further reduction of the supply voltage V_{DD} [1] thanks to a theoretical subthreshold slope (SS) much lower than 60 mV/dec at room temperature. Because of the small bandgap, III-V semiconductors are very attractive as channel material for TFETs. Moreover the on-current may be boosted using heterojunctions and/or strain engineering [2]. Interface states, however, are a serious concern for III-V TFETs [3,4], and may have a large impact on the I-V characteristics.

In this paper we perform a simulation study of n-type and p-type InAs/$Al_{0.05}Ga_{0.95}As$ nanowire (NW) gate-all-around (GAA) TFETs (T1 and T2 respectively, from now on) recently presented in [5], which have shown promising features in terms of SS and I_{ON}. The study is here extended to take into account the effect of traps and strain on the device characteristics, with a full-quantum ballistic transport approach. The trapped charge is calculated with a novel approach, which applies Shockley-Read-Hall (SRH) theory in a way consistent with the ballistic model, without resorting to quasi-equilibrium distributions. The model is used to compute the impact of interface traps, in conjunction with strain.

II. PHYSICAL MODEL

The in-house simulator employed for the present investigation is based on a 4-band **k·p** Hamiltonian [6] to accurately model multiband effects and the complex band structure of our devices. A non-equilibrium Green function (NEGF) formalism is employed for transport description within the ballistic approximation. The effect of strain is included through Pikus-Bir formalism with Bahder extensions [7,8], for zinc-blende crystals.

A. Trap Model

It is assumed that traps are of acceptor type, located at the semiconductor/oxide interface and uniformly distributed over the interface area. The trap energy distribution is modelled on the data presented in [11], in which D_{it} for 10-nm channel length high-k/InAs gate stacks have been reported (traps are within the blue band in Fig. 2). The trap occupation probability is computed through a generalization of the Shockley-Read-Hall (SRH) theory consistent with the ballistic NEGF approach, initially presented in [12] and here extended also to holes. Only the electrostatic effect of traps is considered (through Poisson equation), while transport remains fully ballistic. It is assumed that for each NW cross-section the occupation probability of the traps at each energy in steady state is the result of the balance of the emission and capture processes between such traps and the electronic states belonging to the different NW conduction and valence subbands. The electronic populations injected from the source and drain reservoirs are separately considered according to the ballistic assumption. The InAs/$Al_{0.05}Ga_{0.95}As$ simulated devices are almost equal to the optimized devices used for the TFET inverter analysis carried out in [5]. Both devices were designed to meet the ITRS OFF-state current specifications at V_{DD} = 0.4 V, with sub-60 mV/dec minimum and average subthreshold slope, together with relatively high ON currents. The devices are based on a GAA geometry with square cross section.

III. DISCUSSION OF RESULTS

The turn-on characteristics at V_{DS} = 0.4 V are reported in Fig. 1 for T1 and T2, with and without traps, and with and without 0.5 GPa biaxial tensile strain applied in the plane of the device cross-section (see Fig. 1). In Fig. 2 currents are V_G-shifted to match the I_{OFF} = 100 nA/μm value at $V_{GS,OFF}$ = 0 V. Currents with traps (red squares) are smaller than the ideal ones (black circles), but still steadily increasing with V_{GS}, which indicates that the Fermi-level pinning condition in the channel is not reached for the biases considered here The current reduction is ~60% for T2, and ~20% for T1.

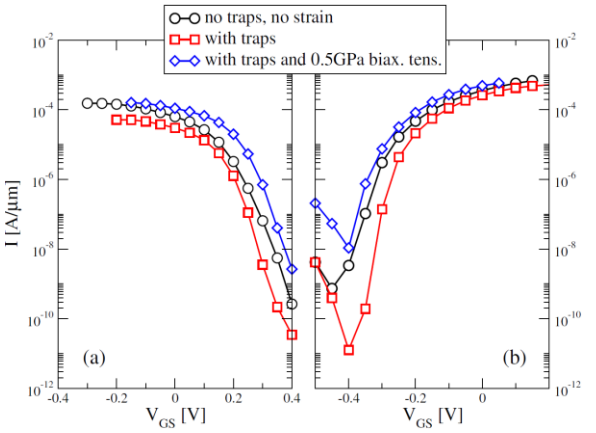

Figure 1. I_{DS} versus V_{GS} at V_{DS} = 0.4 V with and without interface traps, and with and without uniform biaxial tensile strain of 0.5 GPa along the cross-section of the nanowire. (a): T1, (b): T2. Currents are normalized to the nanowire side.

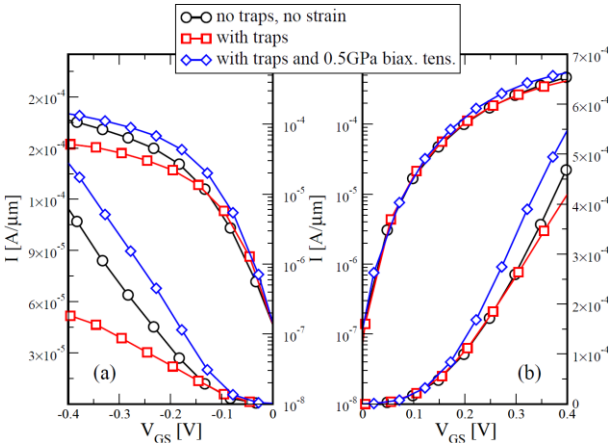

Figure 2. I_{DS} versus V_{GS} at V_{DS} = 0.4 V with and without interface traps, and with and without uniform biaxial tensile strain of 0.5 GPa applied to the NW cross-section. (a): T2, (b): T1. Currents are V_G-shifted in order to have I_{OFF} = 100 nA/µm value at $V_{GS,OFF}$ = 0 V.

The current reduction of unstrained T1 with traps is caused by trapped electrons in the channel that lift up the conduction subband energy, hence increasing the tunnel distance (see Fig. 3, top). One positive drawback of this effect is the electric field decrease at the channel/drain junction responsible for ambipolar behavior. For T2, the situation is different because the trapped charge affects the n+ source region rather than the channel/drain region due to the acceptor type assumed for the traps (Fig. 3, bottom). When biaxial tensile strain is applied, an upward shift of the valence band energy together with a downward shift of the conduction band energy leads to a reduction of the bandgap [12]. We found a bandgap reduction of ~10% for $Al_{0.05}Ga_{0.95}Sb$, and ~15% for InAs. Electron and hole effective masses decrease as well by roughly the same factor as the bandgap. From Fig. 1 we can see that the presence of a uniform biaxial tensile strain of 0.5 GPa not only completely recovers the trap-induced I_{ON} degradation, but also improves I_{ON} and SS (see Table I). Indeed, the band shift induced by a 0.5 GPa biaxial tensile strain is limited and does not cause the facing between channel and drain conduction/valence bands, thus avoiding the onset of undesired channel/drain tunneling paths.

TABLE I. I_{ON}, average SS (SS_{avg}) computed over three current decades, and peak slope (SS_{peak}) extracted from the curves in Fig. 2.

	n-TFET			p-TFET		
	I_{ON} [µA/µm]	SS_{AVG} [mV/dec]	SS_{PEAK} [mV/dec]	I_{ON} [µA/µm]	SS_{AVG} [mV/dec]	SS_{PEAK} [mV/dec]
no strain, no traps	466	40	31	112	59	49
no strain, w. traps	413	40	34	51	49	43
traps and biax. tens.	543	38	31	140	43	41

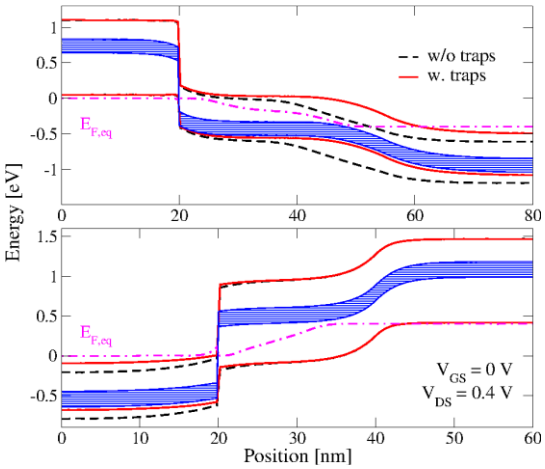

Figure 3. Conduction and valence subbands profile at V_{GS} = 0 V (not shifted as in Fig. 1) for T1 (top) and T2 (bottom), with (solid red) and without (dashed black) traps. The energy interval where trap levels are located has been reported in blue. Magenta dashed curve: equivalent Fermi level $E_{F,eq}$.

IV. Conclusions

Co-optimized p- and n-type TFETs on the same InAs/$Al_{0.05}Ga_{0.95}As$ technology platform have been studied with the aim of investigating the interaction between strain and acceptor interface traps with energy level in the semiconductor bandgap. Traps induce a significant reduction of the ON-current of both devices, as expected. A relatively low biaxial tensile strain uniformly applied to the devices is enough to not only fully recover, but to improve I_{ON} and SS.

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