# Comparative study of non-linearities in 28 nm node FDSOI and Bulk MOSFETs

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***Abstract* — This work investigates, for the first time to our best knowledge, non-linearities in FDSOI MOSFETs and compares them with bulk counterparts. 1st, 2nd and 3rd order I-V derivatives, followed by Harmonic Distortions of 2nd and 3rd order ($HD_2$ and $HD_3$) were extracted based on DC measurements and simulations. Design window (bias conditions) with strongly reduced non-linearity in FDSOI versus bulk was identified and reasons of this reduction are discussed. Application of back-gate bias in FDSOI MOSFET was shown to allow for further improvement of non-linearity.**

***Keywords - Fully depleted (FD) SOI, MOSFETs, non-linearity, harmonic distortion, measurements, simulations***

## I. Introduction

28nm CMOS is considered as a very important node towards mixed digital- RF integration for Internet of Things (IoT) and 5G applications. Amongst planar technologies for 28 nm node, Fully Depleted (FD) SOI process (with ultra-thin-body and buried oxide (BOX) and ground plane (GP)) still co-exists with bulk one. Improved electrostatic, scalability and variability, lower power consumption, better performance in FDSOI MOSFETs w.r.t. bulk counterpart were proved [1]. Comparative studies of self-heating (SH) and its effect on device performance as well as RF Figures of Merit were also reported [2,3]. This work extends for the first time, for our best knowledge, the comparison of these two technologies to the study of non-linearities. Non-linearity is primordial for RF implementations, notably future 5G communication circuits. Drain current in any MOSFET naturally features a non-linear dependence on the applied bias. This is expected to be affected by scaling. Number of effects (e.g. series resistance, $R_{sd}$, short-channel effects (SCE), mobility degradations, velocity saturation, ...) comes into a play complicating non-linearity modeling and making correct non-linear behavior prediction a complex task. Thus, experimental study of non-linearity is a crucial first step needed for the further fair modeling of these effects requested by designers.

## II. Experimental Details

Devices studied in this work come from 28LP bulk and 28FDSOI processes by STMicroelectronics. More process details can be found in [1]. MOSFETs with gate lengths L from 25 to 90 nm were studied. Drain current vs. gate voltage, $I_d$-$V_g$, curves at different drain voltages $V_d$ and $I_d$-$V_d$ curves at different $V_g$ were recorded. In the case of FDSOI these measurements were done at various back-gate biases, $V_{bg}$. To assess non-linearities, 1st, 2nd and 3rd derivatives from these curves were extracted: $g_{m1}=dI_d/dV_g$; $g_{m2}=d^2I_d/dV_g^2$; $g_{m3}=d^3I_d/dV_g^3$; $g_{d1}=dI_d/dV_d$; $g_{d2}=d^2I_d/dV_d^2$; $g_{d3}=d^3I_d/dV_d^3$. Considering a memoryless circuit excited by a sinusoidal signal with AC amplitude A, 2nd and 3rd order harmonic distortions were calculated as $HD_2=A/2|K_2/K_1|$; $HD_3=A^2/4|K_3/K_1|$ with $K_n=1/n!d^nI_d/dV_g^n$.

## III. Results and Discussion

### A. Non-linearities in FDSOI w.r.t. Bulk MOSFETs

Fig.1 shows $I_d$-$V_g$ and $g_{m1}$-$V_g$ curves of bulk and FDSOI MOSFETs in linear and saturation regimes. As expected, the bulk device exhibits a higher subthreshold slope and drain induced barrier lowering (DIBL) than FDSOI one, and thus stronger threshold voltage, $V_{Th}$ reduction with $V_d$. Difference between FDSOI and bulk becomes stronger with $V_d$ increase. This appears also in $g_{m1}$ curves: while the curves are very similar in linear regime, $g_{m1}$-$V_g$ bulk curve stretches w.r.t. FDSOI one at higher $V_d$, due to SCE, $V_d$ dependence of body factor and 2D electric field effect on mobility. $g_{m1}$-$I_d$ curve is an efficient representation to demonstrate these effects (Fig. 2). Advantage of FDSOI w.r.t. bulk counterpart is clear in below-around-$V_{Th}$ region with better $g_{m1}$ at a fixed $I_d$. However, at higher $V_g$ $>V_{Th}+0.2$ V, the curves of bulk devices stretch-out w.r.t. FDSOI ones to higher $I_d$ and $g_{m1}$, whereas FDSOI ones quasi-saturate with $V_d$ increase (particularly at high $V_d$). This may appear similar to $R_{sd}$ effect. However, $R_{sd}$ extracted from RF measurements on the same devices was shown to be lower in FDSOI [3]. Furthermore, $I_d$-$V_d$ curves of these devices (not shown) do not indicate strong difference in $R_{sd}$. Fig. 3a shows that while $g_{m2}$ maximum is lower in bulk devices, $g_{m2}$-$I_d$ curves of bulk devices are stretched to higher $I_d$ (the same is observed for $g_{m2}$-$V_g$ curves, not shown) w.r.t. FDSOI one at higher $V_d$. Or in another words FDSOI curves are compressed w.r.t. bulk ones, thus providing a range of biases/currents where FDSOI features lower $g_{m2}$ w.r.t. bulk. Let's take an

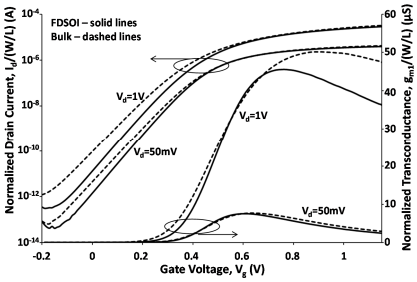


Fig 1. Experimental $I_d$-$V_g$ and $g_{m1}$-$V_g$ curves of FDSOI and bulk devices at $V_d$=50 mV and 1 V. L=30 nm. W=48.6 µm.

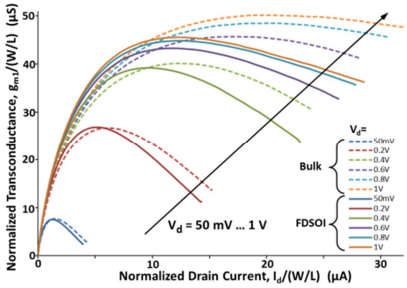


Fig. 2. Experimental $g_{m1}$-$I_d$ curves of FDSOI (solid lines) and bulk (dashed lines) device at various $V_d$. L=30nm. W=48.6 µm.

example of $V_d$=0.8 V and $I_d$/(W/L)=10 µA: $g_{m1}$ of both FDSOI and bulk devices is about the same (see Fig. 2), but $g_{m2}$ is strongly reduced in FDSOI because $g_{m1}$ in FDSOI device is almost saturated under these conditions, whereas it continues to grow in bulk counterpart, thus stretching $g_{m2}$-$I_d$ curves. Similar behavior is observed for $g_{m3}$-$V_g$ and $g_{m3}$-$I_d$ curves (not shown here).

It would be worth pointing out that such difference in $V_d$ behavior of FDSOI w.r.t. bulk devices is not completely reproduced in Spice simulations (see $g_{m2}$-$I_d$ curve in Fig. 3b, other derivatives are not shown due to lack of space). It can be seen that, while low-$V_d$ curves agree well with experiments for both FDSOI and bulk MOSFETs, discrepancy appears at higher $V_d$ for FDSOI device. In fact, "stretched" bulk curves are reproduced well, while "saturation" (quasi–independence on $V_d$) of FDSOI ones w.r.t. bulk at high $V_d$ does not appear in Spice simulations; FDSOI curves behave in the same way as bulk ones.

Silvaco simulations with and without SH (not shown) strongly suggest that the experimentally observed difference in non-linearity behavior between FDSOI and bulk devices is (at least partially) due to SH. Indeed, SH-induced rise of device temperature and related $I_d$ reduction increases with $I_d \times V_d$ and is known [2] to be stronger in FDSOI w.r.t. bulk.

In practice, however, the ratio of $g_{m2,3}$ to $g_{m1}$ is important rather than $g_{mi}$ itself. Fig. 4 plots distortion of 2nd and 3rd order in bulk and FDSOI devices. There exists a clear bias and current conditions at which FDSOI outperforms bulk. It is worth pointing that a $HD_2$ is minimized at lower $I_d$ and $V_g$-$V_{Th}$ (not shown) ranges in FDSOI w.r.t. bulk devices, thus of interest for low-power applications.

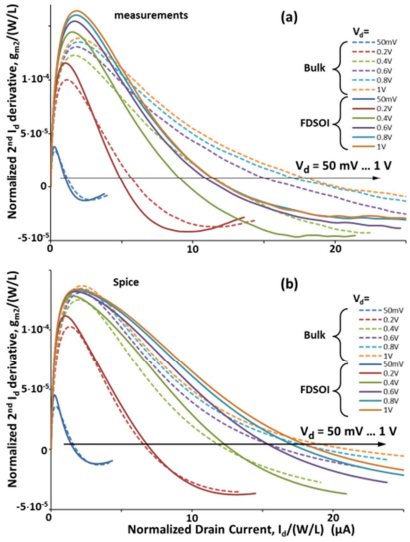


Fig. 3. Experimental (a) and Spice simulated (b) $g_{m2}$-$I_d$ curves of FDSOI and bulk device at various $V_d$. L=30nm. W=48.6 µm.

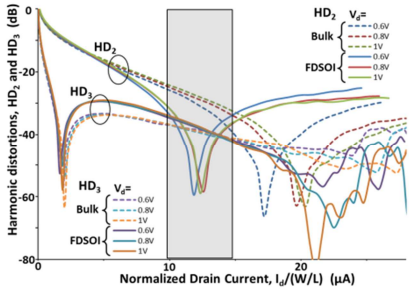


Fig. 4. Experimental $HD_2$ and $HD_3$ vs. $I_d$ curves for FDSOI and bulk. A=0.2 V. L=30 nm. W=48.6 µm. Shaded area gives example of conditions at which FDSOI outperforms bulk.

### *B. $V_{bg}$ effect on non-linearity in FDSOI MOSFET*

Fig. 5 shows $g_{m1}$-$I_d$ curves of FDSOI device at various $V_{bg}$. Application of positive $V_{bg}$ results in the reduction of $g_{m1}$ maximum and global curve flattening. Similar trends are observed for higher order derivatives. These trends can be explained by DIBL and subthreshold slop increase with positive $V_{bg}$ [4], from one side (low $V_g$), and vertical electric field reduction when positive $V_{bg}$ applied, from another side (higher $V_g$). Fig. 6 plots $HD_2$ vs. $I_d$ for various $V_{bg}$. One can see that application of positive $V_{bg}$ may allow for, firstly, further reduction of $HD_2$ in the range where FDSOI already outperforms bulk (at $I_d$/(W/L)=13µA, chosen in the inset in Fig. 6, $HD_2$ reduction is ~20-30 dB) and secondly, extension to higher $I_d$ values (or lower $V_g$, not shown) the range where FDSOI features lower $HD_2$ w.r.t. bulk counterpart.

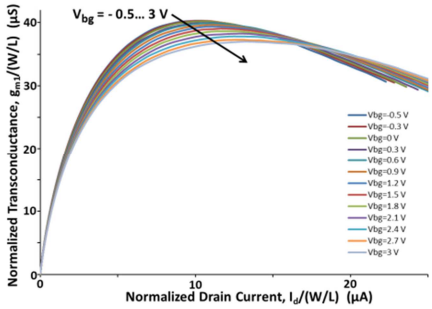


Fig. 5. Experimental $g_{m1}$-$I_d$ curves of FDSOI device at various $V_{bg}$. L=30 nm. W=36 µm. $V_d$=1 V.

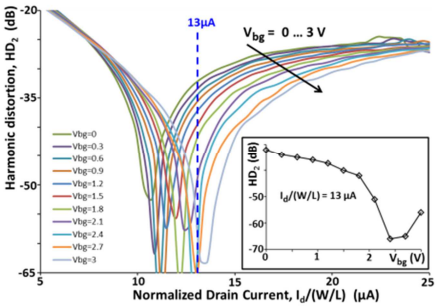


Fig. 6. Experimental $HD_2$-$I_d$ curves of FDSOI device at various $V_{bg}$. $V_d$=1 V. L=30 nm. W=36 µm. Insert gives $HD_2$ vs. $V_{bg}$.

## IV. CONCLUSIONS

Non-linear behavior of FDSOI and bulk MOSFETs was comparatively studied through experiments and simulations. 1st, 2nd, 3rd derivatives of dc $I_d$ as well as $HD_2$ and $HD_3$ were considered. Bias conditions at which FDSOI strongly outperforms bulk counterpart in terms of non-linearity were identified. Worth pointing that minimization of non-linearity appears at lower biases in FDSOI w.r.t. bulk, which is beneficial for low-power applications. Application of positive $V_{bg}$ in FDSOI opens a way for further non-linearity reduction.

## ACKNOWLEDGMENT

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# Sensitivity Analysis of C-V Global Variability for 28 nm FD-SOI

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***Abstract*—This work describes a model for the C-V global variability of 28 nm FD-SOI and analyses the effect of the different process parameters on the measured C-V variability using Leti-UTSOI simulations.**

***Keywords-FD-SOI, split C-V, global variability, Leti-UTSOI, sensitivity analysis***

## I. INTRODUCTION

With CMOS technology scaling to sub-32 nm nodes, the impact of process variability on device performance is gaining importance [1]. A recent work [2] discusses the impact of local and global variability on drain current using a detailed statistical characterization. This work explores the impact of global variability on the C-V behavior of 28 nm FD-SOI devices.

After describing the used experimental setup, the paper proposes a statistical model for the capacitance die-to-die variability. After establishing the validity of the statistics of process parameters extracted from C-V measurements, the contribution of each process parameter to the total variability is quantified using the proposed model.

## II. EXPERIMENTS

Split-CV measurements were performed using Agilent HP407B C-V meter on long-large N channel MOSFETs from the STMicroelectronics 28FD-SOI technology, having front oxide equivalent oxide thickness (EOT) ≈ 1.1 nm, 7 nm Silicon film and 25 nm BOX thicknesses [3]. An AC signal with an amplitude of 25 mV and a frequency of 500 kHz was used in the C-V meter. The front gate to channel capacitance ($C_{gc}$), from all the 114 dies on a wafer, was used for the sensitivity analysis.

## III. STATISTICAL MODELING OF C-V VARIABILITY

Adapting the method in [2] for capacitance, the die-to-die variation quantified by $\sigma^2(\Delta C/C)$, where $\Delta C = C - C_0$ ($C_0$ is the capacitance of die at the center of wafer), can be modeled in terms of the sensitivity of the capacitance to different process parameters as in Table I(1). The sensitivities abs($\partial \ln C/\partial P_i$) for each parameter $P_i$, can be calculated using a model calibrated with the measurement data. The percentage contribution (% $P_i$), defined as Table I(2) can be used to study the contribution of each parameter to the total variability.

## IV. RESULTS AND DISCUSSIONS

The sensitivities obtained from Leti-UTSOI [4] are compared with those obtained from TCAD and Poisson-Schrodinger (PS) solver and is found to be similar (fig. 1a), hence establishing the accuracy of the former.

### A. Validity of statistical extraction

We have already reported methods [5] for the extraction of the front oxide ($T_{ox}$), Silicon channel ($T_{Si}$) and buried oxide ($T_{BOX}$) thicknesses from C-V data. Its ability to reproduce the statistics is verified using Monte Carlo (MC) simulations with Leti-UTSOI, using arbitrary distribution of thicknesses as input. The extracted thicknesses are found to follow the same input distributions (perfect correlation, fig.1b). It is also found to reproduce any correlations between thicknesses used at the input (figs. 1c&d).

### B. Evaluation of the model

The proposed model, Table I(1), is applied to the measured C-V variations. The sensitivities are calculated using Leti-UTSOI model calibrated with the measurement data. Using the standard deviations of the process

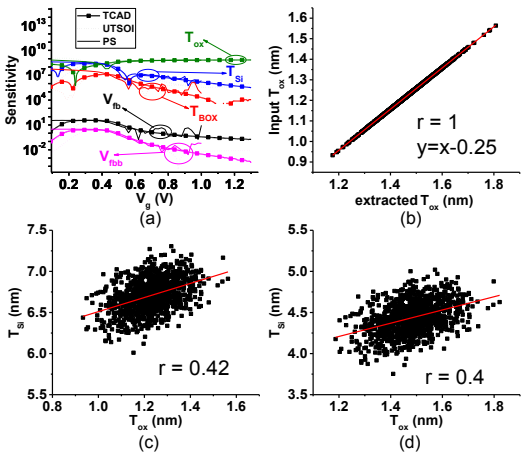



Figure 1. (a) Comparison of sensitivities obtained from different simulators. (b) Perfect correlation observed between input and extracted $T_{ox}$. The offset between input and extracted is due to dark space. Correlation between the (c) input and (d) extracted $T_{Si}$ and $T_{ox}$. Results for NFET.

TABLE I. EQUATIONS USED

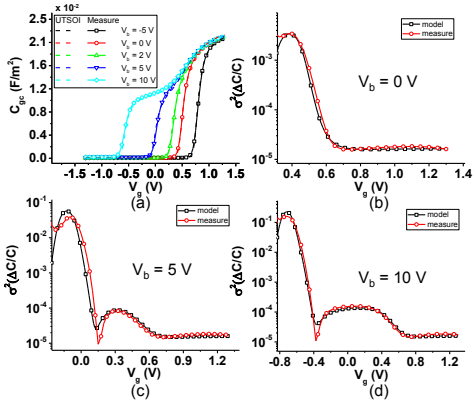
$$\sigma^2(\Delta C/C) = \sigma^2(ln(C/C_0)) = (\partial \ln C/\partial T_{ox})^2\sigma^2(T_{ox}) + (\partial \ln C/\partial T_{Si})^2\sigma^2(T_{Si}) + (\partial \ln C/\partial T_{BOX})^2\sigma^2(T_{BOX}) + (\partial \ln C/\partial V_{fb})^2\sigma^2(V_{fb}) + (\partial \ln C/\partial V_{fbb})^2\sigma^2(V_{fbb}) + (\partial \ln C/\partial W)^2\sigma^2(W) + (\partial \ln C/\partial \ln N_{well})^2\sigma^2(\ln N_{well}) \quad (1)$$

$$\%P_i = \frac{(\partial \ln C/\partial P_i)^2\sigma^2(P_i)}{\sum_i(\partial \ln C/\partial P_i)^2\sigma^2(P_i)} \times 100 \quad (2)$$

parameters ($\sigma(P_i)$) (except flat-band voltages) extracted from measurement as an initial guess, the fitting of the model with measured variations is done at different $V_b$ values. The identification of the dominant contributors at each bias condition, using Table I(2), facilitates the fitting procedure. The $\sigma(P_i)$ of parameters obtained from the fit are close to those extracted directly from C-V measurements (within a maximum error of 25%) (fig. 2).

Percentage contributions calculated with the fitted values of $\sigma(P_i)$ are shown in fig. 3. $T_{ox}$ is observed to be the only dominant parameter in strong inversion, irrespective of the bias applied at the back gate. For very strong forward back biased condition ($V_b$ = 10 V), the effect on $T_{Si}$ becomes quite dominant in weak and moderate inversion, during which the inversion channel shifts from the back to the front interface. On the other hand at $V_b$ = 0 V, the dominant contributor in weak and moderate inversion is the front interface flatband voltage ($V_{fb}$), which is reasonable considering that the inversion is at the front interface. Thus, the dominant contributors at each bias condition can be identified.

The proposed model is shown to fit the measured C-V variability, with the real values of $\sigma(P_i)$ for each process parameter in the technology used. Conversely, together with the percentage contributions, it provides a method to estimate the variance of different process parameters.




| | |
|---|---|
| $\sigma(V_{fb})$ = 1.5 mV | $\sigma(V_{fbb})$ = 1.3 mV |
| $\sigma(T_{Si})$ = 0.13 nm | $\sigma(T_{BOX})$ = 0.11 nm |
| $\sigma(T_{ox})$ = 0.006 nm | $\sigma(W)$ = 1.55 nm |
| $\sigma(\ln N_{well})$ = 0.09 | |

Figure 2. (a) C-V curves obtained from measurement and calibrated Leti-UTSOI model. (b-d) Fitting of the proposed model for the front gate to channel capacitance of an NFET at different $V_b$. The final values of the $\sigma(P_i)$ obtained from the fit is also given.

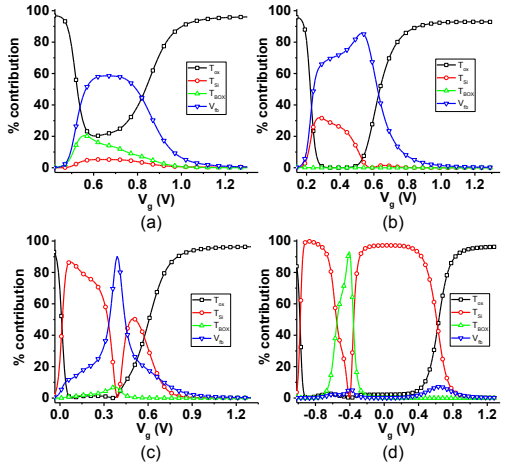



Figure 3. Percentage contributions of the dominant parameters ($T_{ox}$, $T_{Si}$, $T_{BOX}$, and $V_{fb}$) plotted as a function of $V_g$ at (a) $V_b$ = -5 V, (b) $V_b$ = 0 V, (c) $V_b$ = 5 V and (d) $V_b$ = 10 V for NFET.

## V. CONCLUSIONS

The validity of the statistical information extracted using previously reported methods has been verified using Leti-UTSOI simulations. Further, a comprehensive model for the C-V variability in FD-SOI devices has been proposed and verified with the $C_{gc}$ of long large NFET. The proposed model helps estimate the global variability of process parameter and also provides a means to study the contribution of each process parameter to the total variation of the capacitance.

## ACKNOWLEDGMENT

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# Mass data analysis of Random Telegraph Noise in 22nm FDSOI back biased transistors

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***Abstract*—In order to estimate the statistical impact of Random Telegraph Noise (RTN) on integrated circuits the effect has to be analyzed for a large number devices. Therefore a new approach for parallel testing and mass data analysis was introduced. The data analysis is based on fitting Gaussian curves into measurement data based on the Weighted Time Lag Plot (WTLP). The residual error is typically below 3%. Furthermore the influence of Back Gate biasing on the number of active traps for 17400 devices could be shown.**

***Keywords—Random Telegraph Noise; parameter extraction; FDSOI; CMOS; characterization***

## I. INTRODUCTION

With the rapidly evolving Internet of Things (IoT) and RF connectivity, the need has arisen to find a balance of performance, power consumption and cost. The 22nm planar, fully depleted silicon-on-insulator (FDSOI) technology [1] shows promising advantages over 28nm bulk and the three dimensional FinFET technologies. 22nm FDSOI technology offers smaller channel length than 28nm, continuous device dimension scaling compared to FinFET and super low threshold voltage due to the fully depleted feature. It also allows real time threshold voltage adjustment of the MOSFET via Back Gate bias. Therefore 22nm FDSOI is especially well-suited for analog/mixed-signal (AMS) and radio frequency (RF) applications.

In contrast to digital only applications a small noise level can already have severe impact for AMS or RF circuits. That is why all noise contributions have to be understood and modeled. In [1] it is shown that 1/f low frequency noise for 22nm FDSOI is already on par with the ITRS2.0 target. Another low frequency noise component which gained interest in recent years is Random Telegraph Noise (RTN) [2]. Due to the further down scaling FinFET technologies [3] as well as FDSOI technologies [4] are affected.

In this work the RTN of transistors manufactured in 22nm FDSOI are investigated. First the measurement setup and conditions for transistor arrays are described. An algorithm based on the Weighted Time Lag Plot (WTLP) [5] enables reliable RTN detection from the measurement data. In the second part of the paper typical RTN examples are discussed and mass data is presented. Here especially the significant impact of the Back Gate is discussed.

## II. MEASUREMENT AND RTN EXTRACTION

### A. *Measurement setup and conditions*

The characterization is based on a National Instruments (NI) PXI system equipped with source measure unit (SMU) cards. The maximum sample rate for NI SMU cards is 1.8MS/s (600kS/s for the 4 channel cards). For the tests a sample rate of 10kHz with up to 1 million samples for each device under test (DUT) was used. The chassis is equipped with 17 SMU channels in order to enable 8 times parallel testing. The system is easily scalable for higher throughput.

Arrays of standard 4 pad devices are used instead of device matrix arrays (DMA), because DMA structures are not suited for fast measurements [2]. The probe card with 32 needles can test 8 transistors parallel. Separate SMU channels are used for Gate (G) and Drain (D). For the Back Gate (BG) one SMU channel is shared and the Source (S) is connected to ground. This configuration allows individual biasing of each transistor and parallel sampling of the drain current. The noise floor of the measurement setup for the 10 µA current range is well below 1E-24 A²/Hz at 10 Hz (see. Fig. 1.). This includes the PXI system, cables, probe card and prober.

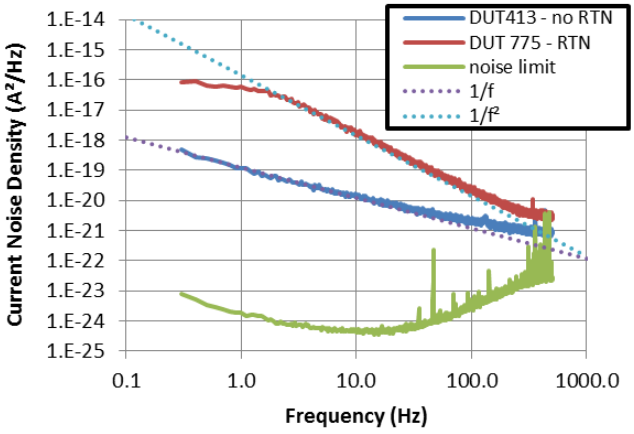


Fig. 1. Current noise density for DUT413 (no RTN) and DUT775 (RTN).

### B. *RTN extraction*

The algorithm is based on a WTLP matrix as shown in Fig. 2. Along the diagonal ID(i) = ID(i+1) the current levels of

interest are visible. In order to improve the statistic for a given element of the diagonal all elements orthogonal to the diagonal are summed up. The result is the curve named Original Signal in Fig. 3 (b). In a second step the algorithm tries to minimize the area below the Original Signal by subtracting Gaussian curves. In this step mainly the magnitude and position (=median) of the Gaussian curves will be optimized. The standard deviation is for all Gaussian curves the same and based on an initial guess from the WTLP.

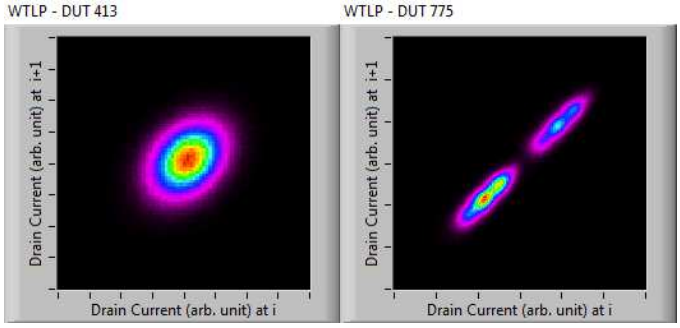


Fig. 2. WTLP for DUT413 with 1 current level detected (no RTN) and DUT775 with 6 current levels detected (RTN).

The algorithm enables reliable detection of multilevel RTN. Fig. 3 (b) shows an example with 6 current levels identified. In the time domain, Fig. 3 (a), only 2 current levels are visible. The other levels are hidden due to other low frequency noise. For DUT775 the remaining difference between the area below the Original Signal and the area below the Superposition of the Gaussian curves is 3% (DUT413: 0.6%, not shown).

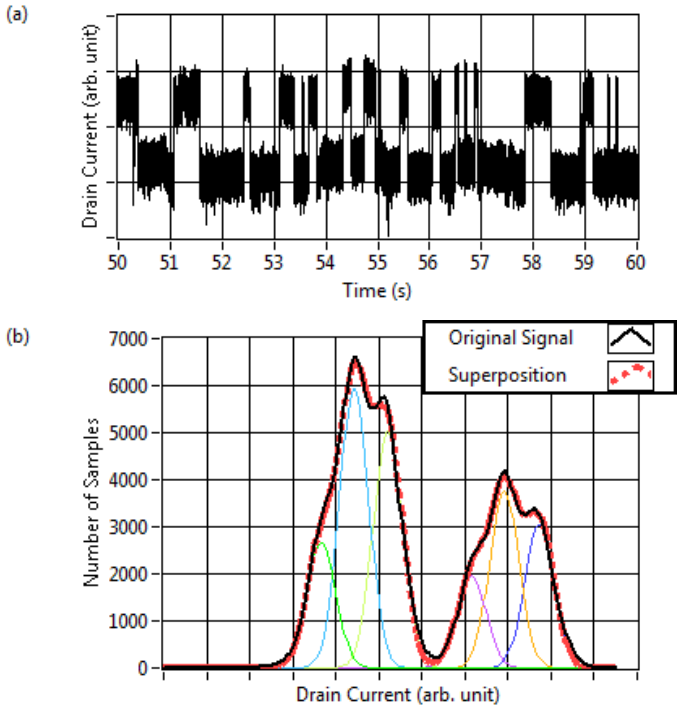


Fig. 3. DUT775: (a) time domain sampling snapshot of the drain current ID showing typical RTN, (b) Good matching of the original signal extracted from the WTLP to the superpositon of all 6 detected current levels.

## III. Back Gate impact on RTN

The algorithm described was applied to test data of 17400 DUT. In order to have the same Drain current for the different BG settings the Gate voltage had to be adjusted. For BG = 0 V only 34.5% DUT show no RTN, whereas for BG = 2 V the number improves to 42.7%. It can be seen in Fig. 4 (b) for more than 3 current levels the semi log plot shows a straight line. This allows to approximate the number of DUT with certain current levels for a given transistor array size.

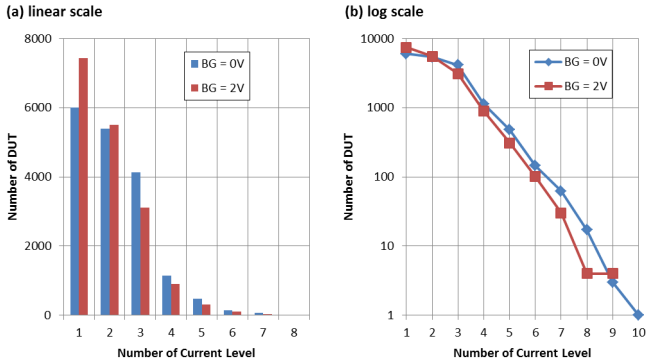


Fig. 4. BG dependent statistic of detected current levels for 17400 DUT measured, plot (a) linear and plot (b) logarithmic scale.

## IV. Summary

RTN of transistors manufactured in 22nm FDSOI was measured with a parallel test approach. This allows recording of mass data, which is then processed by a new algorithm based on the WTLP. Typical RTN examples show the capability of the algorithm. Furthermore it could be shown that the number of current levels and therefore the number of active traps can be influenced by the setting of the Back Gate.

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# Strain-induced increase of electron mobility in ultra-thin InGaAs-OI MOS transistors

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***Abstract*—The impact of strain on electron mobility is investigated in ultra-thin InGaAs-OI channels by combining tight-binding, Schrodinger-Poisson, and mobility simulations. Our model shows that mobility improvement increases with body thickness downscaling, up to 164% in 4 nm-thick InGaAs channels in strong inversion.**

***Keywords—InGaAs-OI; electron mobility; strain; Fermi level pinning; interface charge; ultra-thin body***

## I. Introduction

InGaAs is considered a viable *n*-channel material for future CMOS due to high electron mobility ($\mu_e$) despite e.g. low density of states and Fermi level pinning (FLP) [1,2]. Further enhancement of III-V device performance via transport improvement is possible by applying strain in InGaAs channels [3]. Recently, a strained 15 nm-thick InGaAs-OI MOSFET was reported with a significant $\mu_e$ improvement when tensile strain is applied [4]. In this work, $\mu_e$ in strained, extremely-thin InGaAs-OI channels is analyzed by accounting for bandstructure effects, quantum confinement, and the impact of FLP.

## II. Modeling, Results and Discussion

For $\Gamma$-valley electrons, we employ a nearest-neighbor sp3d5s* tight-binding (TB) approach to calculate the impact of strain on transport effective masses, non-parabolicity factor, and conduction band (CB) minimum shift (TB parameters taken from [5]). The band-structure calculations are validated by the results from [6] (not shown here). Compared to our previous work [7], $\mu_e$ calculations based on MRTA includes the non-linear surface roughness (SR) scattering model from [8] and $N_{it}$ as an additional source of Coulomb scattering (CO). Energy profile $D_{it}$ of interface states in the CB is modeled as acceptor type with exponential distribution: $D_{it} = D_{it}(E_0) \exp[-|(E-E_0)/E_s|])$ (see Table I.).

The calibration of the model is carried out on the experimental data from [4], as reported in Fig. 1 that shows a good agreement between simulations and experiment. The calibration is done by keeping phonon scattering parameters fixed, while $D_{it}$, CO and SR scattering parameters are adjusted (parameters are listed in Table I). As shown in Fig 2(a), CO scattering is the dominant scattering mechanism limiting the total mobility ($\mu_{TOT}$) for $T_B = 15$ nm. Hence, the beneficial effect of tensile strain reported in Fig. 1 clearly comes from the impact of strain on $\mu_{CO}$. The impact of specific CO scattering centers, which includes fixed charge ($N_{int}$), impurity charge ($N_{imp}$) and bias-dependent interface state charge density ($N_{it}$), is plotted in Fig. 2(b). As expected, mobility limited by the bias-dependent charge ($\mu_{IT}$) experiences the most prominent dependence on the inversion charge density ($N_{tot}$). Furthermore, the $\mu_{IT}$ increase due to strain originates from $D_{it}$ energy shift relative to CB minimum in the presence of strain. Fig. 3 reports that the $\mu_{TOT}$ enhancement grows with the tensile strain value ($\varepsilon$) for all $T_B$, in both relatively weak ($N_{tot} = 10^{12}$ cm$^{-2}$) and strong ($N_{tot} = 8\times10^{12}$ cm$^{-2}$) inversions. Moreover, the enhancement increases with $T_B$ downscaling, i.e. up to 164% and 89% in strong and weak inversion, respectively, for $T_B = 4$ nm and $\varepsilon = 1.7\%$. The more pronounced $\mu_{TOT}$ enhancement in thinner InGaAs-OI channels as compared to thicker ones originates from the greater improvement of $\mu_{CO}$ with strain (see Fig 4) at lower $T_B$. When comparing the $\Gamma$-valley ground-state wave-function for $T_B = 4$ nm and $T_B = 15$ nm at $N_{tot} = 8\times10^{12}$ cm$^{-2}$ in Fig 5, the increased sensitivity to strain is observed for $T_B = 15$ nm. Hence, a softer increase of $\mu_{CO}$ and a stronger decrease of $\mu_{SR}$ with increasing strain occur in thicker channels. As strain increases, SR scattering becomes more important, especially for thinnest channels.

## III. Conclusion

We assessed the impact of strain in ultra-thin InGaAs-OI channels. Due to high interface state charge density, $\mu_{TOT}$ is mainly determined by Coloumb scattering. The $\mu_{TOT}$ enhancement is the highest for the highest tensile strain and, moreover, the enhancement is more pronounced for thinner InGaAs channels. For $T_B = 4$ nm, we report the increase of 164% and 89% in strong and weak inversion, respectively. The work shows that the application of strain to InGaAs-OI MOS transistors is more attractive as the scaling progresses.

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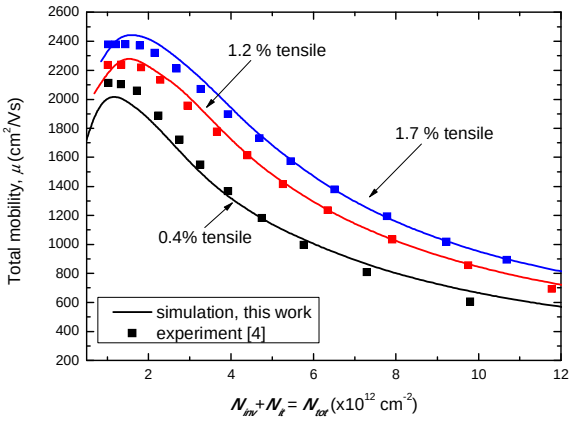


**Fig 1.** Comparison between experimental and simulation data for InGaAs-OI MOSFETs with 0.4 %, 1.2 % and 1.7 % tensile strains. $T_B$ = 15 nm, $T_{ox}$ = 10 nm, $T_{BOX}$ = 30 nm. $Al_2O_3$ is used as GOX and BOX material. Experimental data is taken from [4].

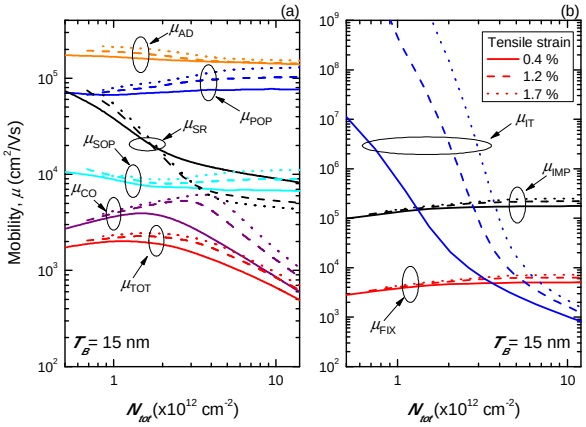


**Fig 2. (a)** Impact of different scattering mechanisms on total mobility as a function of inversion charge density for InGaAs-OI MOSFETs with 0.4 % (solid), 1.2 % (dash) and 1.7 % (dotted) tensile strains. **(b)** Mobility limited by fixed charges as Coloumb scattering centers is designated with $\mu_{FIX}$, by impurity charge $\mu_{IMP}$, and by interface state charge $\mu_{IT}$. $T_B$ = 15 nm, gate and bottom oxides are $Al_2O_3$.

**Table I.** Material and scattering parameters used in self-consistent Schrödinger-Poisson and MRTA mobility simulations.

| 15 nm-thick $In_{0.53}Ga_{0.47}As$ channel | | | |
|---|---|---|---|
| Γ valley | ε (%) | $m_l = m_t (m_0)$ | NP factor α |
| | 0 | 0.044 | 1.3 |
| | 0.4 | 0.043 | 1.3 |
| | 1.2 | 0.041 | 1.35 |
| | 1.7 | 0.039 | 1.4 |
| **Bandstructure and Scattering Parameters** | | | |
| $E_\Gamma$ = 0.75 eV<br>$D_{AP,\Gamma}$ = 7 eV<br>$E_{OP}$ = 32 meV, $D_{OP}$ = 10×10⁸ eV/cm<br>$E_{POP}$ = 32 meV, $\varepsilon_0$ = 13.94, $\varepsilon_\infty$ = 11.64<br>$v_{s,T}$ = 2974 m/s, $v_{s,L}$ = 4253 m/s, $\rho$ = 5506 kg/m³<br>$a$ = 5.868 Å, $V_0$ = 0.5 eV, $N_{imp}$ = 3×10¹⁶ cm⁻³<br>$D_{it} = D_{it}(E_0)\exp[-\lvert(E-E_0)/E_S\rvert])$, $D_{it}(E_0)$ =10¹⁶ eV⁻¹cm⁻²; $E_0$=0.28 eV above CBM; $E_S$ =20 meV | | | |
| **$Al_2O_3$-InGaAs Interface Parameters** | | | |
| (100) | $L$ = 1 nm, Δ = 0.28 nm | | $N_{int}$ = 1.55×10¹² cm⁻² |

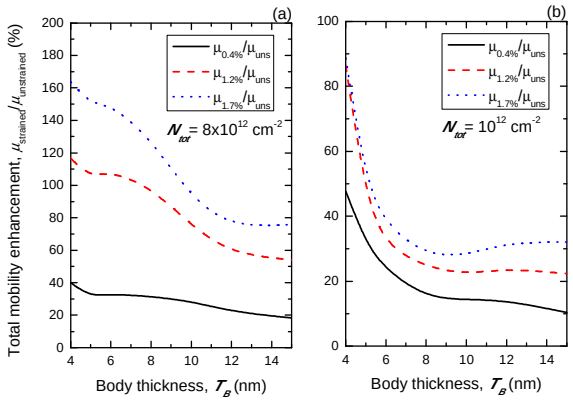


**Fig 3.** Total mobility enhancement as a function of body thickness for 0.4 % (solid), 1.2 % (dash) and 1.7 % (dotted) tensile strains at (a) $N_{tot}$ = 8×10¹² cm⁻² and (b) $N_{tot}$ = 10¹² cm⁻². $T_B$ = 15 nm, $T_{ox}$ = 10 nm, $T_{BOX}$ = 30 nm. $Al_2O_3$ is used as GOX and BOX material.

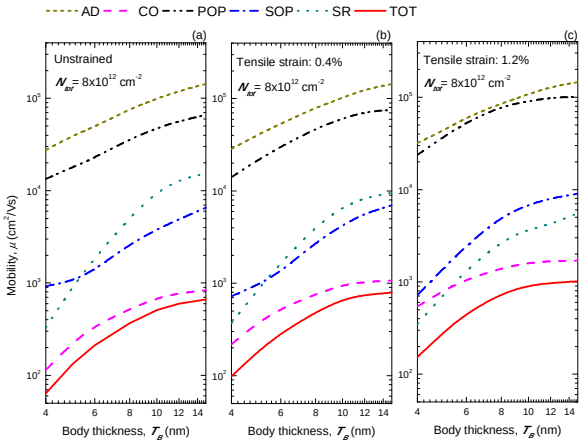


**Fig 4.** Impact of different scattering mechanisms on total mobility as a function of body thickness for (a) unstrained, (b) 0.4 %, and (c) 1.2 % tensile strains. Mobility is extracted in strong inversion, at $N_{tot}$ = 8×10¹² cm⁻². $Al_2O_3$ is used as GOX and BOX material.

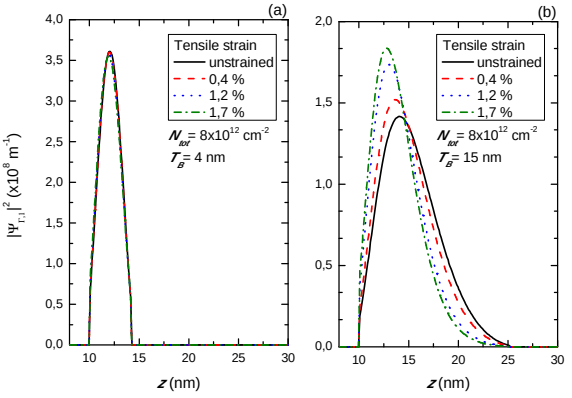


**Fig 5.** $\Gamma$-valley ground-state wave-function for (a) $T_B$ = 4 nm and (b) $T_B$ = 15 nm in strong inversion ($N_{tot}$ = 8×10¹² cm⁻²) for unstrained (solid), 0.4 % (dash), 1.2 % (dot), and 1.7 % (dash-dot) tensile strains.