Compact Modeling of Intrinsic Capacitances in Double-Gate Tunnel-FETs

A. Farokhnejad[1, 2,*], F. Horst[1, 2], M. Graef[1,2], C. Liu[3], Q.T. Zhao[3], B. Iñiguez[2], F. Lime[2], A. Kloes[1]
[1]NanoP, TH Mittelhessen University of Applied Sciences, Giessen, Germany
[2]DEEEA, University Rovira i Virgili, Tarragona, Spain
[3]PGI 9-IT and JARA-FIT, Forschungszentrum Jülich, Germany
[*]atieh.farokhnejad@ei.thm.de

***Abstract*—In this paper an AC-model for a TFET is presented. By means of the carrier concentration and current in the channel, the intrinsic capacitances in a Si Double-Gate (DG) n-TFET are calculated. To verify the model, the results are compared with TCAD Sentaurus simulations as well as measurement data. The model represents a particularly good manifestation of the device AC behavior and is a good estimation of TFET capacitances.**

Keywords- Tunnel-FET; compact model; AC model; intrinsic capacitances.

I. INTRODUCTION

Recently TFETs are in the center of the attractions to be the surrogate of the standard MOSFET. This ever increasing interest owes to their feasibility to overcome the 60 mV/dec subthreshold slope limitation of the standard MOSFETs [1].

In order to allow circuit simulations using multiple TFETs, compact models describing different aspects of the device for all operation regions are necessary. In [2] a DC compact model has been presented. This paper presents a compact model for the intrinsic capacitances in TFETs. The modeled device, is a Si DG n-TFET with a highly p-doped source region N_s=10^{20} cm^{-3}, a highly n-doped drain region N_d=10^{20} cm^{-3} and an intrinsic channel (see Fig. 1).

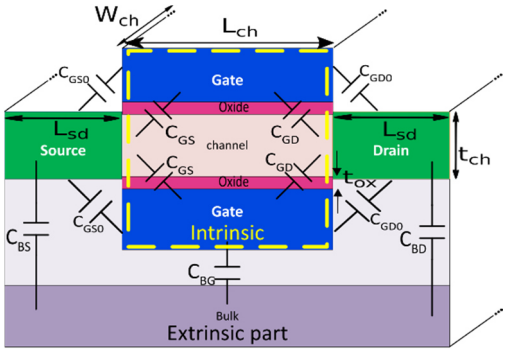

Fig.1. Device geometry and capacitances of a DG TFET. The AC modeling approach focuses on the intrinsic part.

Dimensions of the device are selected as following: L_{sd}=20 nm, t_{ch}=10 nm, W_{ch}=1 µm and t_{ox}=2 nm. Moreover, the high-k oxide material HfO_2 is used in the structure.

The model can also be adapted to p-channel and single gate devices.

II. MODELING APPROACH

The charges which are stored in the transistor yield to a capacitive behavior of the device. Fig. 1 shows the important capacitances in a DG TFET. Here the focus lays on the intrinsic capacitances which are distinct in this figure.

To calculate C_{gd} and C_{gs}, firstly the charge density has to be calculated. In order to do so, it is assumed that the tunneling barrier is the bottleneck for the current flow in the channel. It is also presumed, that in the on-state, this barrier is in distance of $X_{b,s}$ from the source junction and in the ambipolar-state $X_{b,d}$ from the drain junction.

According to these assumptions and considering the inversion charge in the channel region in a multi-gate device [3], the charge density in the channel region at a position with reference voltage V is given as following

$$Q' = 2C'_{eff} V_{th} \alpha \times \mathcal{L}\left(\frac{Q'_{io} \cdot exp\left(\frac{2C'_{eff}(V_{gs}-V-V_0)+Q'_{io}}{2C'_{eff}V_{th}\alpha} \right)}{2C'_{eff}V_{th}\alpha} \right). \quad (1)$$

Where V_{th} is the thermal voltage and α is the slope degradation factor which expresses the ratio between the degraded and the ideal slope in the channel region. Q'_{i0} is the integral inversion charge for an arbitrary gate bias of V_0 in the subthreshold regime [3]. $\mathcal{L}$ is the first branch of Lambert's W function [4]. C'_{eff} represents the effective capacitance including oxide and depletion capacitances in series.

The analysis of long-channel TFETs has shown, that the voltage drop in the channel (ΔV) has to be taken into account. In order to calculate ΔV, firstly the current has to be determined using the DC compact model [2]. Then by multiplying it to the resistivity of the channel between the junction and the tunneling barrier ΔV is obtained. Next, the charge density at the drain junction ($Q'_{d,j}$) and at the barrier ($Q'_{d,b}$) are calculated by solving (1) for V=V_d and V=V_d−ΔV, respectively.

In the same way, just by applying V_s instead of V_d, Q'_s is obtained and the total inversion channel charge associated with source and drain are given as

$$Q_{ch,s/d} = \frac{(Q'_{s/d,j} + Q'_{s/d,b})}{2} W_{ch}(L_{ch} - X_{b,s/d}). \quad (2)$$

Considering the $\Delta Q_{ch,s}$ and $\Delta Q_{ch,d}$ in accordance with changes in source or drain voltage, capacitances are obtained. So in on-state the capacitances are given as

$$C_{gs} = \frac{\Delta Q_{ch,d}}{\Delta V_s} \quad \text{and} \quad C_{gd} = \frac{\Delta Q_{ch,d}}{\Delta V_d} \quad (3)$$

and in ambipolar-state

$$C_{gs} = \frac{\Delta Q_{ch,s}}{\Delta V_d} \quad \text{and} \quad C_{gd} = \frac{\Delta Q_{ch,s}}{\Delta V_d}. \quad (4)$$

III. MODEL VERIFICATION AND CONCLUSION

To inspect the scalability of the AC model, various V_{ds} and L_{ch} are examined. Increasing the drain voltage leads to a shift of the Fermi potential and it lowers the charge attribution to the drain. This is the reason why in Fig. 2 by increasing the V_{ds} the gate-gate capacitance (C_{gg}), which is the summation of C_{gs} and C_{gd}, decreases in the on-state. The longer the channel, the more charges exist in the channel, and thus a bigger capacitance is expected. In Fig. 3 the modeled C_{gs} and C_{gd} are compared with TCAD simulations for different L_{ch}. The model fulfills the expectations and fits very well to the TCAD results.

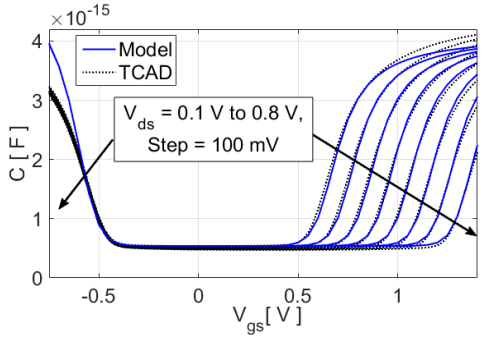

Fig. 2. C_{gg} is compared with TCAD results for various drain voltages. L_{ch}=*22* nm, α=*1.62*, $X_{b,s/d}$ = *3* nm, $V_{0\text{-}gs}$ = *-0.19* V, $V_{0\text{-}gd}$ = *-0.22* V.

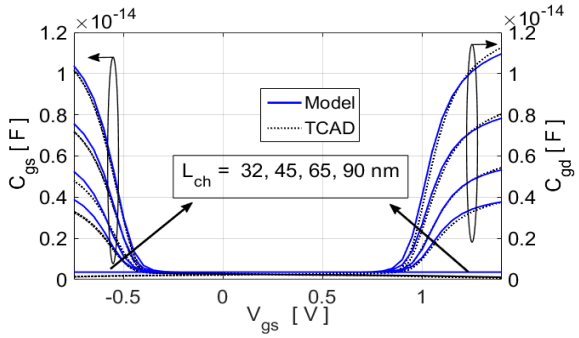

Fig. 3. C_{gs} and C_{gd} are compared with TCAD for various channel lengths. α = *1.53...1.61*, $X_{b,s/d}$ = *3* nm, V_{ds} = *0.5* V, $V_{0\text{-}gs}$ = *-0.19* V, $V_{0\text{-}gd}$ = *-0.22* V.

The model is also compared with measurement data of a p-type single-gate planar TFET. The device dimensions are as following: L_{ch}=*11* µm, t_{ch}=*10* nm, t_{ox}=*5* nm HfO_2 and W_{ch} =*10* µm. In this case, additionally to the voltage drop along the channel, the influence of the parasitic resistances is also included in the model. Along these lines, C_{gs} and C_{gd} are defined as presented in [5].

In Fig. 4 C_{gd} and C_{gs} of the planar TFET, in both on and ambipolar state, are compared with model results. Considering the voltage drop in the channel, in the on-state part of the charges are attributed to the source and in the ambipolar-state they are under the control of the drain [6]. Hence, an increment in C_{gs} and C_{gd} in respectively on-state and ambipolar-state can be seen. The results are in a good agreement with the measurement data as well.

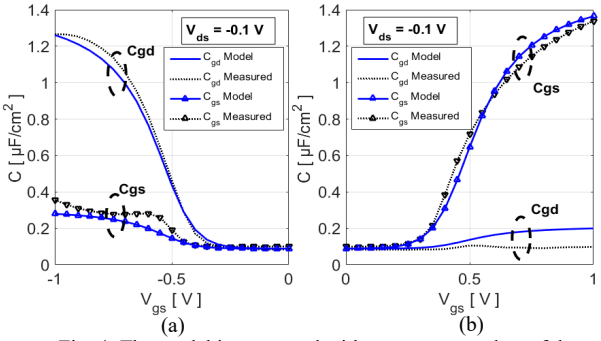

Fig. 4. The model is compared with measurement data of the planar p-TFET: (a) On-state (b) Ambipolar-state. L_{ch}= *11* µm , α=*2.3*, $X_{b,s/d}$ = *3* nm, $V_{0\text{-}gs}$ = *0.01* V, $V_{0\text{-}gd}$ = *0.06* V.

ACKNOWLEDGMENT

This project was supported by the German Federal Ministry of Education and Research under contract No. FKZ 03FH010IX5 and Spanish Ministry of Economy and Competitiveness through project GREENSENSE TEC2015-67883- R. We would like to thank Keysight Technologies for the license donation and support of the software IC-CAP and AdMOS GmbH for support.

REFERENCES

[1] A. C. Seabaugh, and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of IEEE*, vol. 98, no. 12, pp. 2095-2110, 2010.

[2] F. Horst, et al. "Implementation of a DC compact model for double-gate Tunnel-FET based on 2D calculations and application in circuit simulation." *Solid-State Device Research Conference (ESSDERC), 2016 46th European*. IEEE, 2016.

[3] A. Kloes, M. Schwarz, T. Holtij, and A. Navas, "Quantum Confinement and Volume Inversion in MOS3 Model for Short-Channel Tri-Gate MOSFETs," *Electron Devices, IEEE Transactions*, vol. 60, pp. 2691-2694, 2013.

[4] R. M. Corless, G. H. Gonnet, D. E. G. Hare, D. J. Jef and D. E. Knuth, "On the Lambert W Function," *Adv. Comput. Math., vol. 5, pp. 329–359*, Feb. 1996.

[5] T. Smedes, and F. M. Klaassen. "Influence of channel series resistances on dynamic MOSFET behaviour." *Solid-state electronics* 37.2 (1994): 251-254.

[6] C. Liu, et al. "Experimental I–V (T) and C–V Analysis of Si Planar p-TFETs on Ultrathin Body." IEEE Transactions on Electron Devices 63.12 (2016): 5036-5040.

Assessment of Gate Leakage Mechanism utilizing Multi-Subband Ensemble Monte Carlo

C. Medina-Bailon[*1], T. Sadi[2], C. Sampedro[1], A. Godoy[1], L. Donetti[1], V. Georgiev[2], F. Gamiz[1] and A. Asenov[2]
[1]Nanoelectronics Research Group - CITIC-UGR, Universidad de Granada, 18071 Granada, Spain
[2]School of Engineering, University of Glasgow, Glasgow G12 8LT, Scotland, UK
Email[*]: cmedba@ugr.es

***Abstract*— The inclusion in advanced device simulators of quantum effects different than standard confinement becomes mandatory to describe device behavior as technology approaches to nanometer scales. This work presents a model to include Gate Leakage Mechanism considering direct and trap assisted tunneling in Multi-Subband Ensemble Monte Carlo (MS-EMC) simulators. The tool is used for the study of FDSOI and FinFETs.**

Keywords-gate leakage mechanism; direct tunneling; trap assisted tunneling; MS-EMC; FDSOI; FinFET

I. INTRODUCTION

As electronic devices have been scaled down, new transistor architectures are considered to replace standard technology. Currently, FinFETs are being recognized as an alternative to Fully-Depleted Silicon-On-Insulator (FDSOI) devices thanks to their immunity to short channel effects. From a modelling point of view, to explain its behavior, it has been mandatory the inclusion of additional phenomena not needed in previous technological nodes [1]. In particular, the use of ultra-thin insulators, where a high electric field appears, increases the probability of tunneling through the gate oxide. This work presents the development and implementation of this phenomenon known as gate leakage mechanism (GLM) [2] in a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator. The model includes direct and trap assisted tunneling and is applied to compare the performance of FDSOI and FinFETs.

II. METHODOLOGY

The starting point of the simulation frame is the MS-EMC code presented elsewhere [3-4]. The tool, based on the mode-space approach of quantum transport [5], decouples confinement direction and transport plane, where the Schrödinger equation and the BTE are solved, respectively (Fig. 1). Device parameters and orientations for the structures herein analyzed are shown in Fig.1. For the sake of comparison, the trap location inside the gate insulator and its energy have been set equal in both devices, in opposition to standard variability studies where they are randomly distributed. Five different kinds of events considered as GLM are depicted in Fig.2: direct tunneling from the substrate to the gate (i), elastic (ii) and inelastic (iii) tunnel into a trap, tunnel from the trap to the substrate again (iv), and finally from the trap to the gate (v). The GLM is implemented as a stochastic mechanism evaluated for each superparticle after a Monte Carlo flight. The model depends on the position of the carrier in the device and specific parameters related to the tunneling phenomena. In particular, the WKB approximation is used to evaluate transmission coefficients for direct tunneling similar to [6]. In the case of trap assisted tunneling, trap occupation obeys Pauli's exclusion principle and energy-dependent phonon absorption-emission is considered in the inelastic cases. The implementation of the model and its inclusion in the MS-EMC flowchart are shown in Fig. 3.

III. RESULTS

The differences in the orientation of the considered devices modify the electron distribution and the carrier confinement effective mass (m_z*). In this study, m_z* for the most populated valley is higher for the FDSOI compared to the FinFET. As a result, the transmission coefficient is higher for FinFETs. However, this fact is compensated by the volume inversion effect which concentrates the charge distribution in the center of the channel (Fig. 4), reducing the total tunnel probability respect to FDSOI devices as shown in Fig. 5. It is necessary to emphasize some other remarks in Fig. 5: i) direct tunneling is the dominant phenomenon due to the ultra-thin oxide; ii) available states are required for a trapped electron to return to the substrate and so this process becomes forbidden as the gate bias increases. Finally, Fig. 6 shows the impact of GLM on the relative variation of drain current compared to the ideal case without leakage ($\Delta I_D/I_{D,W/O}$) as a function of V_{GS}. As observed, all devices increase the leakage while biased in subthreshold region. However, GLM has a smaller impact on FinFETs when channel thickness is reduced being a better candidate for future ultra-low power applications.

REFERENCES

[1] H.-S. Wong, IBM Journal of Research and Development, vol. 46, 2002.

[2] Y. Taur and T. H. Ning, Cambridge University Press, "Fundamentals of Modern VLSI devices", chap. 2, 2009.

[3] C. Sampedro, F. Gámiz, A. Godoy, R. Valín, A. García-Loureiro and F.G. Ruiz, Solid-State Electronics, vol. 54, pp. 131–136, 2010.

[4] C. Sampedro F. Gámiz and A. Godoy, Solid-State Electronics, vol. 90, pp. 23–27, 2013.

[5] R. Venugopal, Z. Ren, S. Datta, M. S. Lundstrom and D. Jovanovic, .J Appl Phys., vol. 92, 2002.

[6] C. Medina-Bailon, C. Sampedro, F. Gámiz, A. Godoy and L. Donetti, Solid-State Electronics, 2016. In press

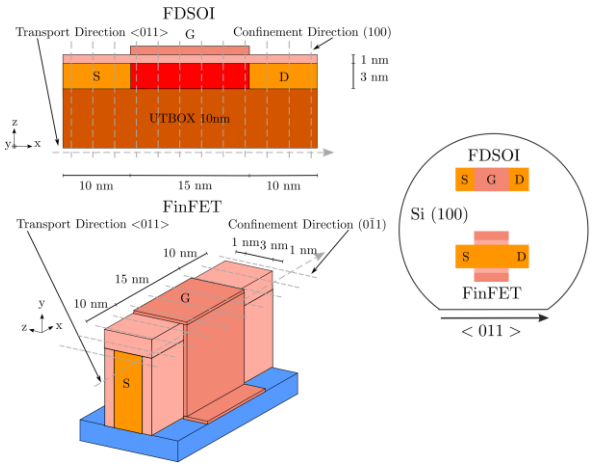

Figure 1. FDSOI and FinFET structures analyzed in this work with L_G=15nm. 1D Schrödinger equation is solved for each grid point in the transport direction and BTE is solved by the MC method in the transport plane.

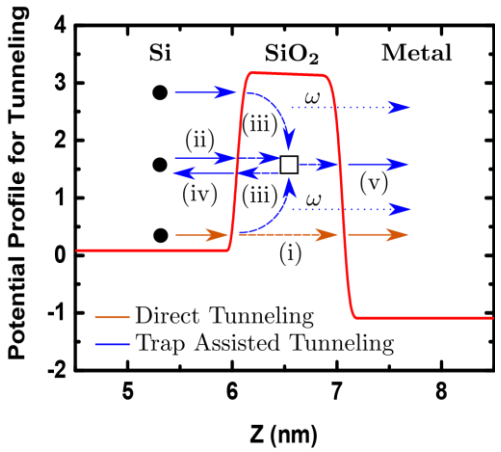

Figure 2. Schematic band diagram of a MOS structure with metal gate and silicon substrate where transport mechanisms implemented in the MS-EMC simulator are described: (i) direct tunneling, (ii) elastic and (iii) inelastic tunneling into a trap emitting or capturing a phonon with energy ω, (iv) detrapping to the substrate, and (v) tunneling from the trap to the gate.

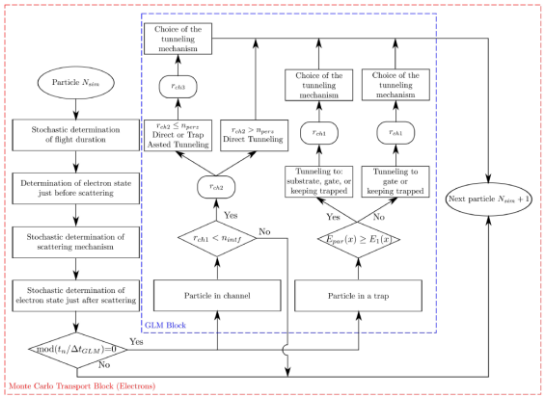

Figure 3. Schematic description of the inclusion of the GLM block in the general flowchart of the MS-EMC tool.

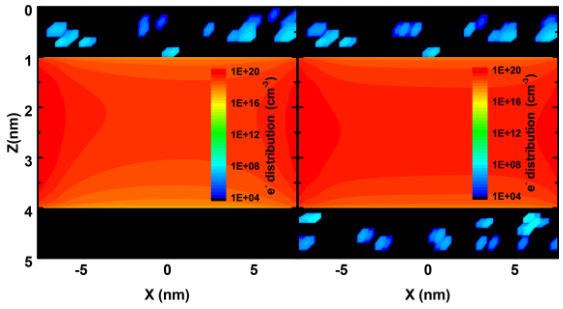

Figure 4. Electron distribution in the channel region including GLM for FDSOI (left) and FinFET (right) with T_{Si}=3nm, V_{GS}=0.6V and V_{DS}=100mV.

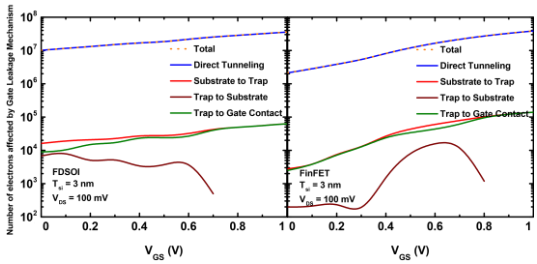

Figure 5. Average number of electrons in arbitrary units affected by each phenomenon and the total GLM as a function of V_{GS} with T_{Si}=3nm at low V_{DS} for FDSOI (left) and FinFET (right).

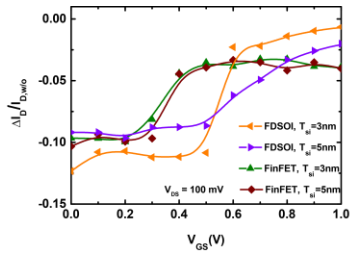

Figure 6. Ratio of the drain current variation to the drain current without taking into account GLM ($\Delta I_D/I_{D,W/O}$) as a function of V_{GS} for FDSOI and FinFET at low V_{DS}.