Investigation of InAs/GaSb tunnel diodes on SOI

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***Abstract*— Tunnel diodes are of interest to gain insights into the limitations of tunnel FETs (TFETs) as they enable us to distinguish effects of the heterojunction from device parasitics found in a three terminal device. Here, we report on InAs/GaSb nanowire heterojunction tunnel diodes monolithically integrated on silicon-on-insulator substrate (SOI). The nanowires were grown using template-assisted selective epitaxy (TASE). Temperature dependent I-V measurements show a change in the conductance slope due to the presence of defects at the heterojunction. Comparison with TFETs shows a similar temperature dependence of the slope, but with smaller absolute values. We further performed room temperature pulsed I-V measurements on the same diodes to analyze traps contribution and we observed no significant dependence on pulse time down to 10µs.**

Keywords-III-V; diode; nanowire; TFET; conductance slope; tunnel;

I. INTRODUCTION

The tunnel field effect transistor (TFET) is a promising solid-state switch for ultra-low power operation [1-2]. TFETs are based on band-to-band tunneling (BTBT) which is very efficient in InAs/GaSb heterojunctions because of the broken band alignment combined with the small effective tunneling mass. Investigation of two-terminal diodes is useful to understand the impact of the junction band alignment and heterojunction defects, as non-idealities related to gating and oxide traps may be neglected. Agarwal et al. [3] introduced the conductance slope (C_{slope}) concept, in analogy to the subthreshold swing (SS) of a TFET. This quantity allows to correlate the negative differential resistance (NDR) region of a tunnel diode to the reverse bias region of a TFET. Although quantitatively different the steepness of both provides a measure of the interface quality and the impact of traps. Here we fabricate and characterize n^+-n-p^+ InAs/GaSb tunnel diodes and discuss their behavior.

II. EXPERIMENTAL RESULTS

The InAs/GaSb nanowire tunnel diodes investigated in this work are fabricated on SOI substrates using TASE. A schematic of the process flow is shown in Fig. 1, main fabrication steps are reported in detail elsewhere [4-5]. The p-n-n+ (GaSb/InAs/InAs) diodes were grown by metal-organic chemical vapor deposition and the nanowire cross section is 30nm×80nm. The estimated doping levels are $4{\cdot}10^{18}$ cm^{-3} for the n^+-InAs, $1{\cdot}10^{17}$ cm^{-3} for the unintentionally doped InAs and low $5{\cdot}10^{17}$ cm^{-3} for the p-GaSb. STEM analysis of the heterointerface on measured diodes is shown in Fig. 2. Fig. 3 shows temperature-dependent measurements. The C_{slope} improves from 221 mV/dec at 300K to 62 mV/dec at 150 K while the peak-to-valley current ratio (PVCR) increases from 2,3 to 3.4. The temperature dependence of the C_{slope} indicates that impurities are limiting the steepness of the tunneling mechanism at the heterojunction. Compared to previous diode structures from our group [6], the C_{slope} is three times steeper at room temperature due to an increased doping level. Fig. 4 compares the C_{slope} of diodes to SS of TFETs from [7]: both improve with decreased temperature, but C_{slope} of the new diodes is significantly steeper. A benchmarking of InAs/GaSb tunnel diodes reported up to now is shown in Fig. 5. Pulsed I-V characteristic is shown in Fig. 6a. Pulsing can reduce the contribution of some parasitic tunneling mechanisms which is expected to lead to a lower excess current. However, an apparent improvement in C_{slope} is only detected in few devices (Fig. 6b) and needs more investigations. The low absolute current of the single nanowire devices limited the ability to go to higher frequencies, which can be circumvented by using nanowire arrays in the future. Finally, a first attempt to investigate the effect surface passivation on diode characteristic is shown in Fig. 7 by comparing two batches of p-n diodes with and without the SiO_2 template. Further experiments using diodes from the same batch are needed to verify that the differences are dominated by surface effects.

III. CONCLUSION

In conclusion, we have investigated the electrical properties of monolithically integrated InAs/GaSb tunnel devices. Analysis of the temperature dependence of the C_{slope} and of the PVCR reveals that defects at the heterointerface are limiting performance similarly to TFETs, but that C_{slope} is steeper than SS.

ACKNOLEDGMENT

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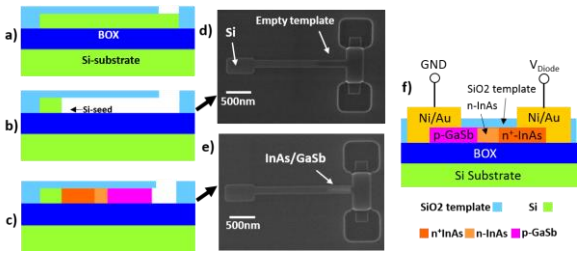

Figure 1. Process flow of n^+-n-p InAs/GaSb diodes fabricated by TASE. Schematics of a) Si nanowires covered by SiO_2 template b) TMAH Si etch-back, c) III-V grown by MOCVD, d-e) SEM top-view of step b-c), f) Finished device including contacts.

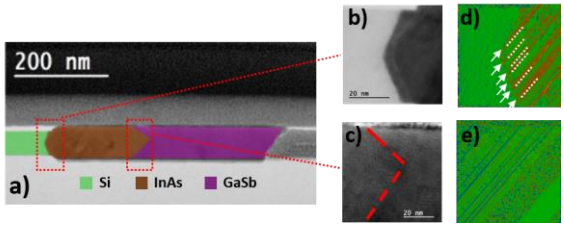

Figure 2. STEM images of InAs/GaSb hetero-structure from [6]. a) Lateral bright-field false colored STEM image of the nanowire. Magnification of the b) Si/InAs interface, c) InAs/GaSb interface, and corresponding GPA d), e). A V-groove <111> shape of Si is seen in b), as well as the presence of misfit dislocations highlighted with white arrows at the Si/InAs nucleation interface d). The InAs/GaSb interface is characterized by presence of planar defects propagating over the GaSb segment e).

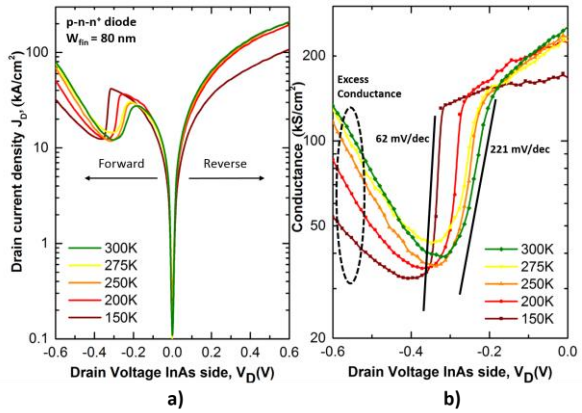

Figure 3. Temperature dependent electrical measurement of a p-n-n^+ diode with nanowire width 80 nm. a) I-V characteristic in semilog-scale. b) Absolute conductance vs. applied bias from the same diode. For 300 K and 150 K plots an average conductance slope is extracted from I_{peak} to I_{valley} and marked by black bars.

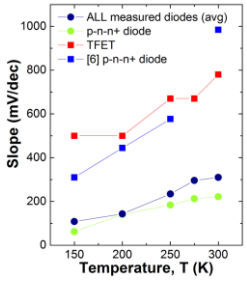

Figure 4. Comparison of the C_{slope} trend with the temperature for the diode in Fig. 3 (green line), average of all the measured diodes (blue line), diode reported in [6] (light blue line), with the SS trend of the InAs-GaSb n-TFET in [7] (red line).

Ref.	Growth	Substrate	Geometry	NDR	J_{peak} [kA/cm²]	PVCR
[8]	MOVPE	GaAs	50 nm vertical nanowire	yes	67.0	2.1
[9]	MBE	GaSb	1 μm² area	yes	500.0	3.4
[10]	MBE	GaAs	0.875 μm² area	no	-	-
[11]	MOCVD	GaSb	InAs film, 10μm diam.	yes	12.0	1.1
This work	MOCVD	Si	80 nm horizontal nanowire	yes	26.6	2.3

Figure 5. Benchmark for InAs/GaSb based tunnel diodes with focus on key technology parameters, i.e. PVCR, peak current density and integration on Si. Our tunnel devices are monolithically integrated on Si and compared to other works they have lower current densities but good PVCR.

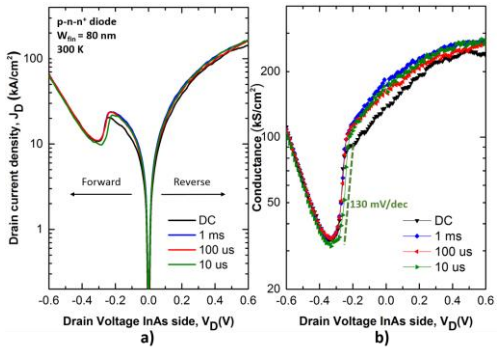

Figure 6. Pulsed I-V measurement of a p-n-n+ diode with nanowire width 80 nm. a) I-V characteristic in semilog-scale. b) Absolute conductance vs. applied bias of the same diode. The characteristics show a slight improvement in PVCR (1.92 to 2.27) and independent slopes for this device.

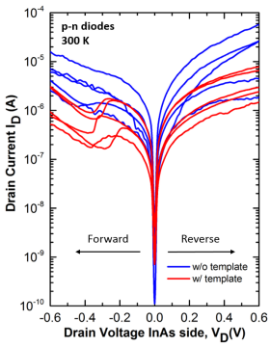

Figure 7. I-V characteristic in semilog-scale of different p-n^+ diodes with the template (red lines) and without the template (blue lines). The devices without the template are not showing NDR. The two device types have been fabricated from two different runs.

On the electron velocity-field relation in ultra-thin films of III-V compound semiconductors for advanced CMOS technology nodes

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***Abstract*—We report Multi-Valley-Multi-Subband Monte Carlo simulations of the velocity-field curves in bulk and thin film InAs, GaAs and $In_{0.53}Ga_{0.47}As$. Our model suggests that surface roughness scattering reduces the saturation velocity of nanometer-scale films significantly below the corresponding Silicon value. The injection velocity, instead, remains larger than for Silicon down to small film thickness. The results provide a useful reference for the calibration of TCAD compact models.**

Keywords—III-V compounds, velocity-field, Multi-subband Monte Carlo

I. Introduction

Ultra-thin films of compound semiconductors represent a promising option for the fabrication of nanoscale nMOSFETs with high injection velocity at scaled CMOS nodes [1]. The calibration of TCAD compact models for ultra-thin III-V semiconductor films is still difficult, due to scarce experimental data on fundamental transport properties. In fact, state of the art technologies have not yet reached full maturity, and electron transport is often much affected by defects, border and interface traps. To mitigate this difficulty, we present an extensive study of electron drift velocity-electric field (v_d-F) characteristics in bulk and thin film III-V semiconductors, suited to support the calibration of TCAD transport models for ultra-thin films.

II. MV-MSMC model

We use a multi-valley, multi-subband Monte Carlo transport model (MV-MSMC) for electrons in III-Vs [2,3] that extends considerably our previous simulator for Silicon transistors [4,5]. Wavefunction penetration in adjacent materials and a consistent non-linear surface roughness scattering (SRS) model are implemented [6].

The MV-MSMC model features a non-parabolic effective mass approximation (NP-EMA) of the bands; parameters are extracted from Tight Binding calculations as described in [8].

Fig.1 compares calibrated MV-MSMC simulations of drift velocity (v_d) in thick bulk-like InAs, GaAs and $In_{0.53}Ga_{0.47}As$ layers. InAs has the largest peak v_d. Notice that our simulations do not account for impact-ionization (II), that may be large in InAs due to the small bandgap. According to [9], II-induced intervalley electron transfer yields a second v_d peak ($\approx 8\cdot 10^7$ cm/s) at F≈100 kV/cm.

III. V_D-F curves in ultra-thin films

Following the calibration on bulk samples, we use the MV-MSMC model to simulate the v_d-F curves of UTB-DG structures with uniform field and T_W=4 and 7 nm, which are realistic values for L_G=10 and 15 nm nMOSFETs, respectively [10]. Thin films free of surface and border traps are considered. SRS parameters have been calibrated on measured mobility for $In_{0.53}Ga_{0.47}As$ inversion layers [11]; we assume they are the same for all three materials. In particular, Δ_{rms} (0.3 nm in this study) is larger than for a Silicon/gate dielectric interface (0.21 nm), but reflects state-of-the-art III-V technology [7]. We also neglect extrinsic sources of scattering due to remote phonons and charges in the high-k gate dielectric. The calculated v_d should thus be regarded as an upper limit for an idealized thin film. **Fig.2** shows the v_d-F curve for $In_{0.53}Ga_{0.47}As$ according to three models: w/out SRS and screening due to free carrier (FCS), with SRS but no FCS and with SRS and FCS. **Fig.3** summarizes the results for InAs and GaAs with phonons, SRS and screening.

All materials exhibit a reduction of the peak v_d for decreasing T_W, even if SRS is not active. In fact, for all materials the confinement induced by smaller T_W modulates the transport mass of the Γ valley; furthermore, it reduces the Γ-L valley separation, which especially in GaAs increases the population of low velocity L-valleys. SRS remarkably lowers the velocity peak and, especially for T_W=4 nm, the low field mobility as well. For T_W=7 nm, the v_d-F curve is sensitive to N_{INV} due to a changing shape of the potential well. The effect vanishes at T_W=4nm where size-induced confinement dominates. We also see that v_d-F curves deviate significantly from the corresponding bulk ones if SRS is included, while the effect of screening is negligible.

Fig.4 (left) shows the v_{sat} at $N_{INV}=5\cdot 10^{12}$ cm^{-2} and F=20 kV/cm for InAs, $In_{0.53}Ga_{0.47}As$ and F=70 kV/cm for Silicon films as a function of T_W. Interestingly, in spite of the substantially higher peak v_d of bulk InAs w.r.t. $In_{0.53}Ga_{0.47}As$, at such large fields the latter material has higher v_{sat} than InAs over most of the T_W values. This trend does not consider II at high fields that could lead to even higher v_{sat} but, however, would be detrimental for device operation. Furthermore, for the chosen Δ_{rms} the III-V curves fall below the Silicon ones at small T_W. The right plot reports the injection velocity, v_{inj}, i.e. the velocity attainable at the virtual source in a ballistic transport regime. The v_{inj} decreases as T_W is scaled, mainly due to the increased transport mass [8]. However, v_{inj} remains much larger than for silicon down to the smallest explored T_W. The potential advantage of ultra-

thin body III-V nMOSFET over the Silicon ones is thus confirmed.

IV. Conclusions

The v_d-F characteristics in Figs.2 and 3 are, to the best of our knowledge, the first published set of such calculations for thin films in III-Vs, and represent a useful reference for the calibration of the corresponding TCAD models of field dependent mobility.

Acknowledgments

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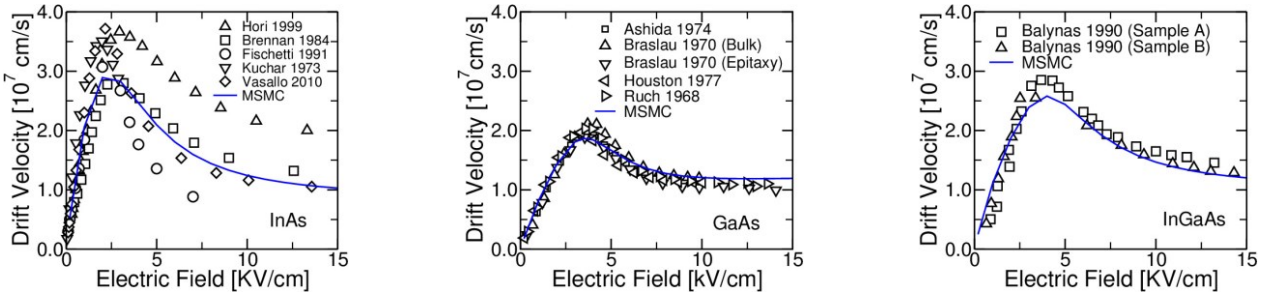

Fig. 1. Electron v_d-F curves in bulk InAs (left), GaAs (center) and $In_{0.53}Ga_{0.47}As$ (right). MV-MSMC simulations of thick layers exhibiting quasi-bulk behavior are compared to simulations and measures from literature. Phonon and alloy scattering are included in the simulations.

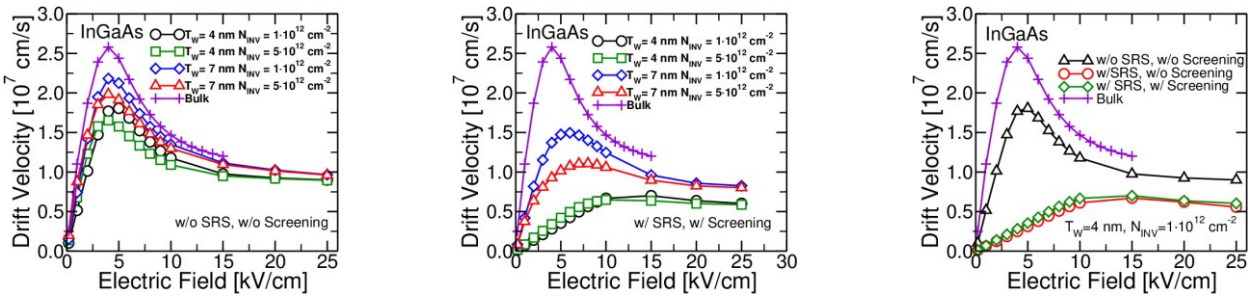

Fig. 2. Electron v_d-F curves in trap-free $In_{0.53}Ga_{0.47}As$ DG MOSFETs with T_W=4 and 7 nm. Left: including phonon and alloy scattering. Center: including also SRS with screening. Right: importance of the different scattering mechanisms. The bulk case is shown for reference.

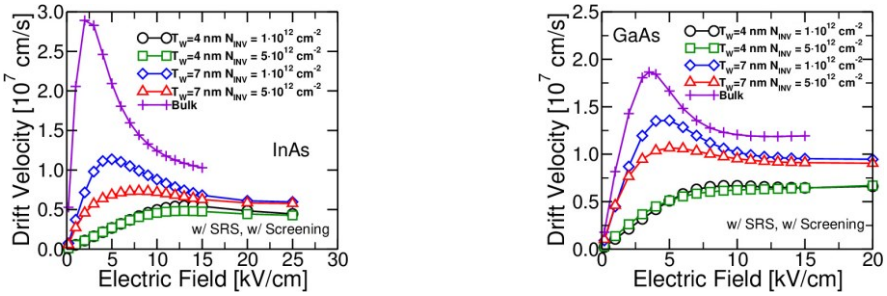

Fig. 3. v_d-F curves including phonon and SRS for DG MOSFETs with T_W=4 and 7 nm and InAs (Left) or GaAs (Right) channels.

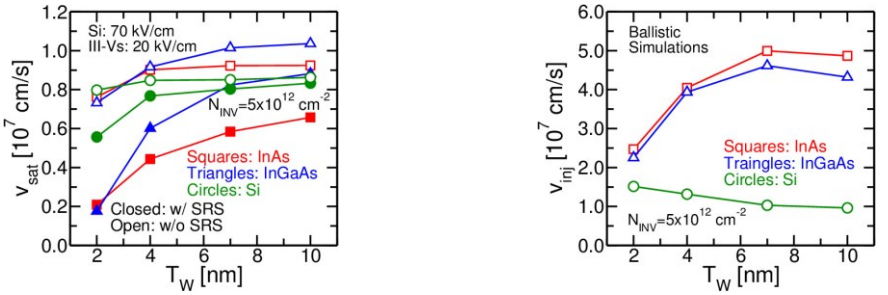

Fig. 4. Simulated saturation velocity (Left) and injection velocity (Right) versus T_W for InAs, $In_{0.53}Ga_{0.47}As$ and Silicon.

GaN-On-Insulator: From QDs to a new substrate

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***Abstract*— RF MBD technique was used to deposit GaN QDs and polycrystalline films on SiO_2. This approach paves the way for easy and versatile fabrication of GaN-On-Insulator materials for future logic and non-volatile memories devices based on heterogeneous III-V/Si integration.**

Keywords- gallium nitride; nanocrystals; non-volatile memories; quantum dots; silicon-on-insulator

I. INTRODUCTION

Silicon-On-Insulator technology offers currently one of the most promising substrates for future nanoelectronics [1]. Over the years, this technology has triggered researchers worldwide to focus on the fabrication of "Semiconductor-On-Insulator". In this research context, many interesting new substrates for integrated circuits have been presented such as SiC-On-Insulator, Germanium-On-Insulator, and sSi-On-Insulator. A milestone in this effort was the SmartCut technology based on which any semiconducting thin film materials can theoretically be transferred on an insulator. However, for a successful application of the method, the existence of the transferred semiconductor on another substrate is required. This prerequisite increases significantly the cost of the final new substrate. The situation is becoming more difficult when the fabrication of the transferred semiconductor is implemented through an expensive process, such as molecular beam epitaxy (MBE).

Here, we present a method to deposit GaN material on thin SiO_2 layers grown on Si substrate. We demonstrate that the formation of GaN quantum dots (QDs) on SiO_2 films by Radio Frequency plasma assisted Molecular Beam Deposition (MBD). By increasing the GaN dose, which is measured in equivalent monolayers of GaN, we found that a very thin continuous polycrystalline GaN layer can be achieved, suitable for the formation of GaN nanodevices on insulator. The samples with GaN QDs were tested as possible candidates for nonvolatile memories [2].

II. EXPERIMENTAL

On 100mm n-Si (100) wafers (1-2 Ω.cm), 3.5 nm thick SiO_2 was grown by dry oxidation at 950 ^oC in standard atmospheric pressure furnace. Subsequently, GaN QDs were formed on the SiO_2 films RF-MBD. In this approach, the materials for deposition are supplied in the form of molecular beams, oriented to the substrate, under high vacuum conditions, as in the case of typical MBE. Gallium atoms and active nitrogen species were supplied using a Knudsen cell and a RF plasma source, respectively. To investigate the formation of GaN material on SiO_2, we implemented samples with different GaN deposited doses (in monolayers, ML) by varying the deposition time. One ML is the material dose that corresponds to one monolayer of (unstrained) epitaxial GaN, grown along the (0001) axis. Samples with 5, 8, 10, 14, and 18 GaN MLs were fabricated. For the sake of comparison and in order to investigate the effect of nitrogen plasma on the quality of the oxide, one reference sample was exposed to the RF plasma nitrogen beam but in the absence of any Ga atoms supply. A reasonable device to study and take advantage of the GaN QDs memory was the memory capacitor, where the 2-D arrays of QDs are covered by a 20 nm thick SiO_2 (TEOS) layer deposited by LPCVD at 710 ^oC. Al was used for gate and back-contact electrode.

III. RESULTS & DISCUSSION

The fabricated samples were investigated by AFM and TEM. The memory capacitors were characterized in terms of charge storage and retention.

A. Surface and Structural Characterization

The formation of GaN QDs on the SiO_2 layers was first examined by tapping mode AFM (Fig.1, inset). These studies were done together with c-AFM measurements. Specifically, the c-AFM tip (Pt/Ir) was located on the SiO_2 and next on top of a QD and I-V curves were measured. Evidently, the I-V exhibited a significant hysteresis due to the injection and rejection of electrons under the proper bias polarity (Fig.1).

Fig.2 presents the cross-sectional HRTEM micrographs for samples with 5 MLs and 18 MLs. It should be emphasized that the process steps we employed to fabricate the thin poly-GaN layer can be used to integrate GaN devices with CMOS circuits. Moreover, horizontal

GaN NW-FETs on insulator seems to have better performance compare to Si due to the higher dielectric constant of GaN, i.e the physical length λ is reduced about 20%.

B. Electrical Characterization

- Comprehensive investigation of the memory capacitors was performed [3]. In Fig.4 the retention of the programing state is presented for all samples. Obviously, the 5 MLs sample can retain its programming state for >10 yrs. With increasing of the density of QDs the trapped charge leaks laterally moving from dot to dot (see Fig.3). The good retention for the 5MLs sample is due to the negative conduction band offset of GaN QDs compare to Si, i.e. $E_{C,Si} - E_{C,GaN} = -0.7$ eV [3].

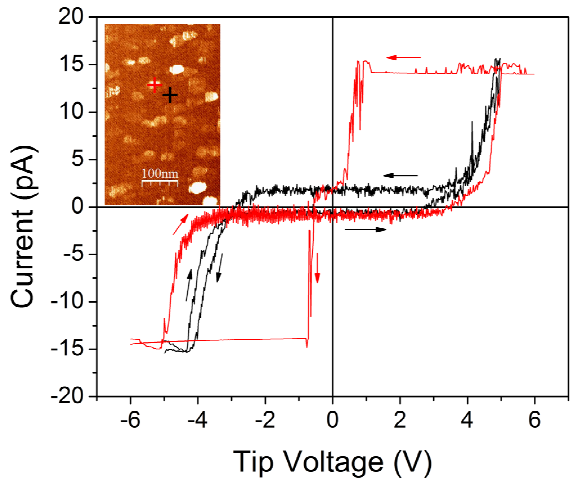

Figure 1. Conductive AFM measurements on sample with 5 MLs GaN on SiO_2. The inset denotes the areas on the topography image of the sample where the I-V curves were measured.

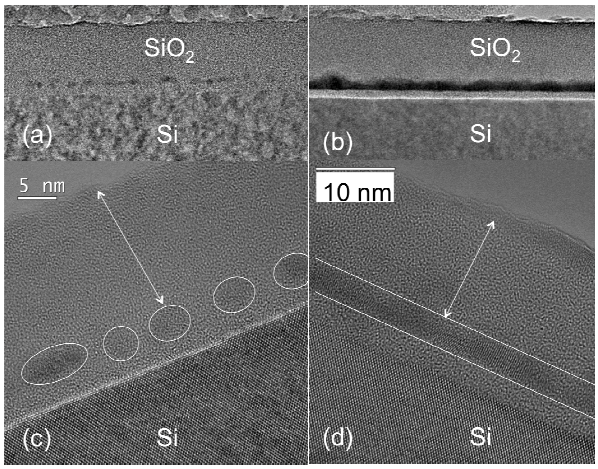

Figure 2. (a)-(b) Bright Field cross-sectional and (c)-(d) high-resolution TEM micrographs for the samples with 5 MLs and 18 MLs.

In conclusion, we have demonstrated that GaN material can be deposited by RF MBD on SiO_2 in the form of QDs up to a thin polycrystalline film. The latter could be used as a new CMOS compatible GaNOI substrate for heterogeneous integration.

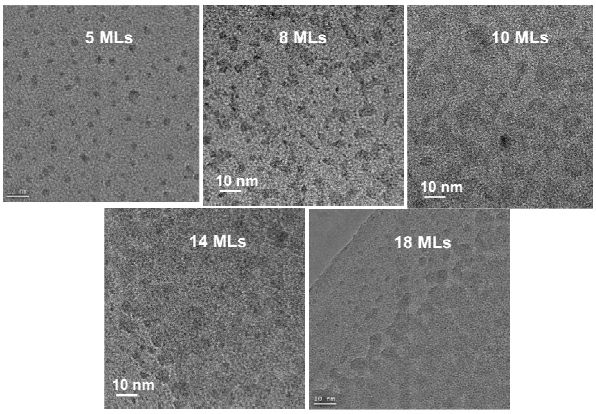

Figure 3. Plan view TEM micrographs denoting the evolution of a polycrystalline GaN layer with dose increase.

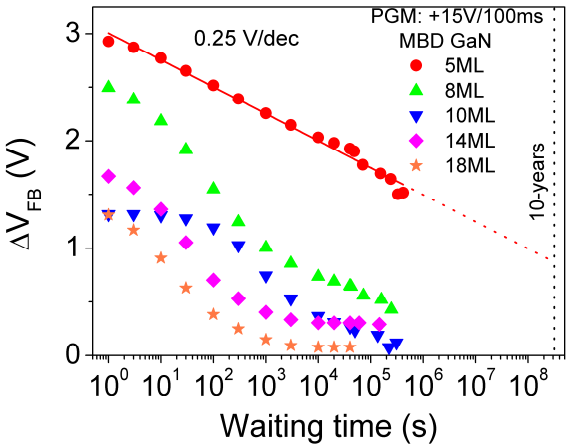

Figure 4. Retention characteristics of the fabricated samples measured at room temperature after electron charging by a pulse voltage +15V/100ms

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Modeling the Impact of 2D Hole Gas in a GaN/AlGaN/GaN Heterostructure

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In this paper, we present a physics-based model to explain the effect of a thick GaN cap layer on the two-dimensional electron gas (2DEG) density and the surface barrier height in a GaN/AlGaN/GaN heterostructure by including the effect of a 2D hole density of states.

AlGaN/GaN high electron mobility transistors (HEMTs) are promising candidates for future high power as well as high frequency applications. These III-V nitride based devices have been a topic of research over the last decade because of their interesting properties like wide band gap signifying a higher breakdown voltage, high electron mobility, and a high saturation drift velocity. The presence of the 2DEG ~10^{13}cm^{-2} at the AlGaN/GaN interface has been observed, and its formation is attributed to the high spontaneous and piezoelectric polarization present coupled with the surface states [1, 2]. Now, one can use a GaN cap layer at the top of the AlGaN/GaN heterostructure in order to build HEMT devices for Normally-off operation. In our previous work [3], we have shown a physics-based model to explain the variation of the 2DEG and the surface barrier height (SBH) by including the surface donor states in such a GaN/AlGaN/GaN stack. However, the impact of the 2D hole gas (2DHG) on the resultant electron concentration was not considered. The influence of the 2DHG is non-negligible when the GaN cap is relatively thick. Here we include the effect of the valence band (VB) to explain the impact of the 2DHG on the resultant electron density n_s and the SBH ($q\cdot\Phi_B$).

The band diagram of the GaN/AlGaN/GaN heterostructure is shown in Fig. 1, where the formation of the 2DHG is highlighted. The different parameters are: $q\cdot\sigma$ is the spontaneous and piezoelectric induced polarization charges at the AlGaN/GaN interface [1] (C/cm^2), ε is the AlGaN dielectric permittivity, E_F is the difference between the Fermi level and the conduction band (CB) minimum at the GaN hetero-interface (eV), ΔE_C is the CB offset (eV), E_d is the surface donor level (eV), n_0 is the constant surface donor density (cm^{-2}eV^{-1}), E_g is the band gap, and F_1 (F_2) is the electric field in GaN cap (AlGaN). Fig. 2 shows the charges at the various interfaces. The charge neutrality condition is maintained throughout the stack, and we show how the 2DEG is formed at AlGaN/GaN interface from two distinct sources, (**i**) the surface donor states present at the GaN cap top given by the n_0 and E_d parameters, (**ii**) the generated electron leaving behind the hole at the GaN cap/AlGaN interface.

In order to find the necessary mathematical expressions, we find $F_2 = \dfrac{q\phi_B + F_1 d_{cap,GaN}}{d_{AlGaN}}$ from electrostatics and by ignoring E_F. To maintain the continuity of displacement at the GaN cap/AlGaN interface, we can write (c.f. Fig. 1) $\varepsilon F_2 = q\sigma - \varepsilon F_1 - q.D_h(q\phi_B + F_1 d_{AlGaN} - E_g)$ and thereby include the effect of 2DHG density of states D_h~$(1.5\cdot q\cdot m_0)/(\pi\hbar^2)$, where m_0 is the electron rest mass. At the AlGaN/GaN interface, one can also write $F_2 = \dfrac{q(\sigma - n_s)}{\varepsilon}$. By combining these equations, one can deduce an expression of n_s (which includes the term $q\cdot\Phi_B$ as well). The simplified form, when $d_{cap,GaN}$ is sufficiently high ($d_{cap,GaN}\rightarrow\infty$), is $n_s = \sigma - \dfrac{E_g\varepsilon}{qd_{AlGaN}} \Big/ 1 + \dfrac{\varepsilon}{qD_h d_{AlGaN}}$. Fig. 3 shows the modeled value of n_s for a wide range of $d_{cap,GaN}$. The experimental data [4, 5] is very close to our previous theoretical prediction [3] for lower values of $d_{cap,GaN}$. However, the model [3] fails when $d_{cap,GaN}$=228nm, and the experimental data shows close agreement with our above mentioned expression of n_s including D_h. The variation of n_s with d_{AlGaN}, when the GaN cap is very thick, is shown in Fig. 4. The discrepancy between the experimental points and the theory

may have been caused due to: (**i**) we ignored the value of E_F for simplification (**ii**) we approximated $d_{cap,GaN} \rightarrow \infty$ (**iii**) we did not consider any trap charge effects. Nevertheless our model can closely predict the experimental observations. Now, as n_s is formed from two sources, $n_s = n_0(q\phi_B - E_d) + D_h(q\phi_B + F_1 d_{AlGaN} - E_g)$. One must solve these set of equations to obtain n_s and $q \cdot \Phi_B$ individually. The analytical expression is cumbersome, nevertheless our model can also approximately predict the variation of $q \cdot \Phi_B$ with d_{AlGaN} (Fig. 5).

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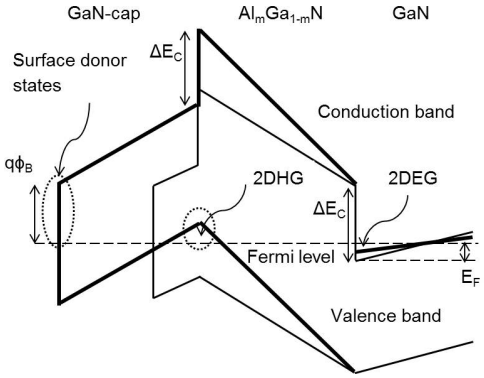

Fig. 1. Band diagram of the GaN/AlGaN/GaN heterostructure is drawn, showing the formation of 2DEG at AlGaN/GaN interface.

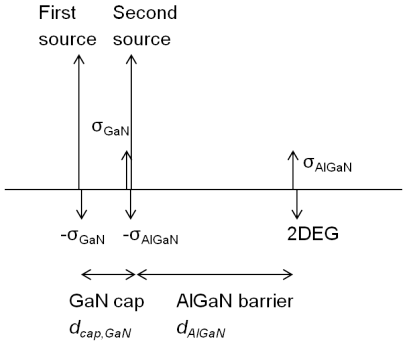

Fig. 2. Schematic shows the sheet charge densities at different interfaces, and the sources of 2DEG formation.

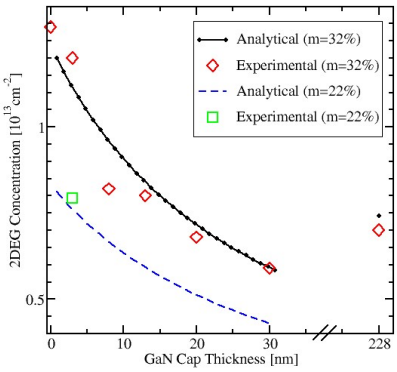

Fig. 3. The modeled 2DEG value of the GaN/AlGaN/GaN heterostructure is shown. The surface state parameters are fitted to the Hall experimental points reported in [4] (for m=0.32, d_{AlGaN}=20nm) and [5] (for m=0.22, d_{AlGaN}= 23.4nm).

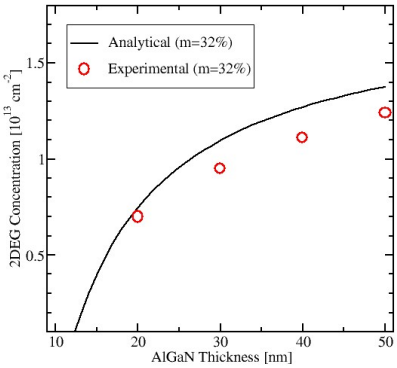

Fig. 4. The 2DEG variation with d_{AlGaN} when GaN cap thickness is as high as 228nm is shown. The Hall experimental data is taken from [4].

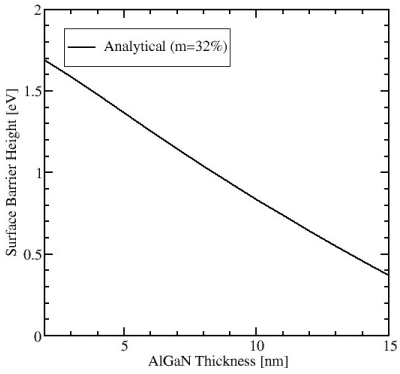

Fig. 5. The approximate variation of the SBH is shown for a GaN/AlGaN/GaN stack with 228nm GaN cap.