The mystery of the Z^2-FET 1T-DRAM memory

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***Abstract*— We review the operation mechanisms of the Z^2-FET underlining its attractiveness as a capacitorless DRAM memory. The main parameters that govern the memory performance are discussed based on systematic experiments and simulations.**

Keywords-Z^2-FET; SOI; band modulation; carrier lifetime.

INTRODUCTION

Band-modulation devices have recently been proposed for sharp switching, ESD protection and memory [1-8]. They are conceptually different from MOSFETs although the same technology, namely FDSOI, is used. The simplest variant is the Z^2-FET structure which is actually a PIN diode with large gate underlap. It is similar to a TFET, but operated in forward-bias mode. Electrostatic barriers are formed (via gate disposition and biasing) to prevent electron/hole injection into the channel until the gate or drain bias reaches a turn-on value. The front and back gates induce electrostatic doping in the undoped body so the device looks like a P+NPN+ thyristor, although the mechanisms of operation differ. The gate action leads to band modulation along the channel subject to a positive feedback mechanism, able to abruptly switch the device (< 1 mV/decade) from OFF state with low leakage current to ON state with high drive current. The output I-V characteristics exhibit a large hysteresis useful for single-transistor memory (1T-DRAM) applications.

In the first part, we will present experimental results and discuss in detail the device physics, architecture, and processing steps of the Z^2-FET. The rationale for developing Z^2-FET, 1T-DRAMs will be presented by referring to the limitations of other types of floating-body memories that rely on the co-existence of electron and holes layers within the body. In ultrathin FDSOI devices, this coexistence is denied by the super-coupling effect. In contrast, the Z^2-FET is free of super-coupling and operates successfully even in sub-10 nm thick films. The Z^2-FET memory is unrivalled in terms of retention time, memory margin and non-destructive reading. Another advantage is the full compatibility with the FDSOI process, without any additional technology module needed. The memory performance will be documented by systematic measurements revealing the roles of gate/anode bias, program and read pulses, temperature and geometrical parameters. We will demonstrate low-voltage operation with ~1 V read bias and program bias as low as 0.4 V. These assets make the Z^2-FET very attractive for high-speed embedded memory applications.

The memory mechanism is rather subtle. It is clarified with numerical simulations that offer guidelines for the development of physics and compact models. We will discuss the avenue for device scaling and optimized operation. Alternative designs for enhanced performance will be presented.

ACKNOWLEDGMENTS

This work is being supported by the European project REMINDER.

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Feasibility Demonstration of New e-NVM Cells Suitable for Integration at 28nm

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***Abstract*— *Abstract*— Memory cell selection for 28 nm and beyond and its integration into new eNVM technology have been investigated through atomic layer deposition (ALD) HfO_2 resistive memory devices. Both amorphous and crystalline HfO_2 layers exhibit promising switching characteristics. It was shown that more than 3 times less power is required to activate the memory device fabricated using the amorphous layer. The forming voltages for both of the memory cell are greater than 10 Volt relative to layer thickness. As an alternative potential resistive memory element, SiOx layer formed on n and p type Si wafers exhibited interesting forming features.**

Keywords-Resistive RAM; HfO2; style; e-NVM; 28nm

I. INTRODUCTION (HEADING 1)

In line with the trends in emerging semiconductor manufacturing and application requirements, higher density, low power consumption, high speed and reliable memories are demanded by industry. It is still not clear if the shrink of the e-Flash beyond 28nm node will be technically feasible and cost effective. In this context, in recent years, research in the memory fields has generally converged in the approach of a two terminal memory resistive device located at the cross point of two conductor lines, as phase change memory (PCRAM), metal oxide resistive switching memory (OxRRAM), conductive-bridge memory (CBRAM) or magnetic memories (MRAM). In particular, main advantages of these technologies are the low voltages, fast read/write, good scalability and low cost.

This work is devoted to the exploration of possible alternatives to the standard Flash memory cell. In fact the presence of high-k in the 28 nm logic with the standard Flash device architecture seems to be a serious hurdle to the development of a product with standard FEOL Flash. The reliability of Flash memories integrating high-k materials has to be proved for the stringent requirements of industry such as automotive of smartcard market. Our objective is to define the most suitable embedded non-volatile memory (NVM) cell to be integrated in the quite complex 28nm and below CMOS platform. It is not possible to anticipate right now, which will be the selected cell, but very likely it will be in the resistive RAM field including OxRAM and PCRAM in this field. To address the best RRAM candidates for the 28nm technology node, MRAM solution can be added. In any of these selections, one should define the main characteristics of the candidate cell, both in terms of process steps and reliability needs. The selection of the cell will require the development of elementary test structures as well as more complex test vehicles at technology nodes. Advanced technology nodes definitely beyond 28nm, for example the development of 14nm and 10nm memory cell structure should be considered under the complexity of the advanced CMOS nodes with the new NVM cell architecture.

II. TECHNOLOGICAL DETAILS

HfO2 layers grown 300mm Si by Atomic Layer Deposition (ALD) were investigated by optical, structural and electrical measurements of memory devices. The role of defects and their nature are beeing investigated on test samples. 50nm Pt by e-beam evaporation followed by RTA annealing at 400 oC 30min in nitrogen atmosphere

SiOx cells were fabricated by surface treatment of wafers using HF:HNO3. Thickness, metalization and annealing dependent forming was observed on SiOx cells on Si. Defects and microstructure have been determined by XRD, Raman and FTIR measurements. Room temperature current-voltage characteristics have been carried out using a semiconductor parameter analyser.

III. RESULTS AND DISCUSSION

Investigation of HfO2 as candidate memory cell revealed interesting properties. Two sets of wafers were examined with the one having an amorphous phase and the second wafer exhibits orthorhombic and monochlinic phases as evidenced from XRD studies. Localized and phonon modes have been observed and attributed to Hf-O phonons and Si-Cl at 770cm^{-1} and 520-570cm^{-1}, respectively, where angle of incidence measurements confirm the phonon mode origin of the band at around

760 cm^{-1} shifting to 770cm^{-1} at 60^{o} incidence. Presence of Chlorine atoms can favor amorphous or polycrystal growth and formation of Si-Cl bonds in hafnia.

The results on switching devices fabricated using 50 nm ALD grown crystalline and amorphous HfO2 layers of 50nm thick indicate that more than 3 times less power is required to activate the memory device fabricated using the amorphous layer. The forming voltages for both of the memory cells are greater than 10 Volt due to relatively high layer thickness (50 nm). Differences in forming voltages are due to compliance current settings which were resulted in to incomplete forming.

Current-voltage characteristics showing reset currents in SiOx based resistive device is indicative of forming at initial sweep. I-V characteristics of a SiOx memory cell on N+Si(100) wafer annealed by RTP at 400^{o}C 30min under N_2 have lower forming voltages. A negative differential resistance effect region is shown following the electroforming process in an untreated SiOx device. Above max, the resistance starts to increase, which results in a decrease of current. At larger voltages, it starts increasing again due to resistance saturation.

IV. CONCLUSION

Resistive memory cell devices have been investigated as potential candidates for 28 nm technology node. HfO2 and SiOx based memory cells both amorphous and crystalline were the subject of studies. ALD deposited amorphous HfO_2 layer exhibited promising switching properties, having more than 3 times less power to activate the memory device which can be the most desired cell structure for 28nm technology. The effect of down-sizing in dimensions and the effect of metallization will certainly enable us to optimize the device characteristics leading to a final decision on the cell selection. As an alternative resistive memory element, SiOx layer formed on n and p type Si wafers by vapour etching exhibited interesting forming features at relatively low forming energies.

ACKNOWLEDGMENT

This work was supported by PANACHE project ENIAC Nanoelectronics under contract≠621217.

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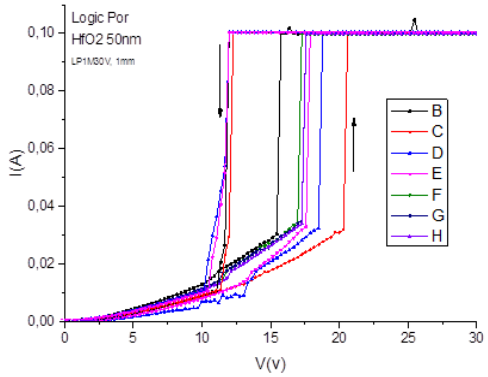

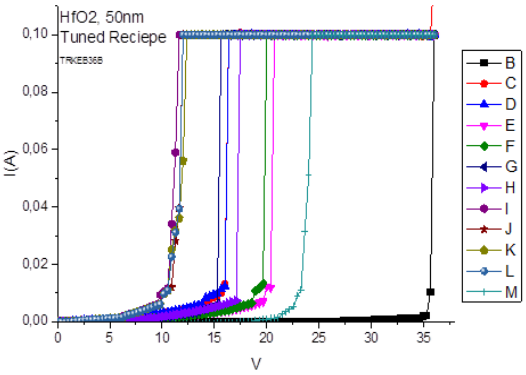

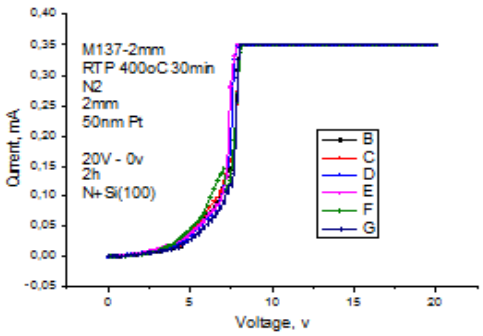

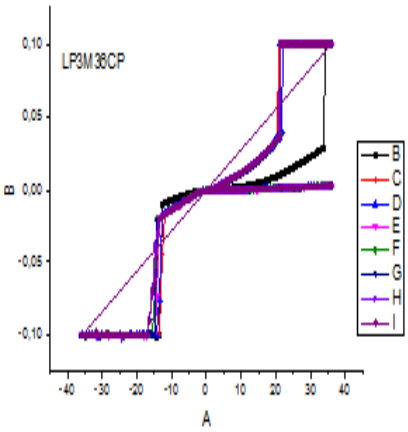

Impact of carrier lifetime on Z^2-FET operation

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***Abstract*—A systematic study to model and characterize the band-modulation Z^2-FET device is developed. Emphasis is given on the effect of carrier lifetime which is the key parameter. It provides guidelines to design Z^2-FETs for sharp switching, ESD protection and 1T-DRAM applications. We provide new insights of the relation between carrier generation/recombination and electrostatic barriers.**

Keywords-Z^2-FET; SOI; band modulation; carrier lifetime.

I. Introduction

Z^2-FET, a partially gated PIN diode, is one amongst the family of sharp-switching devices that has shown excellent applications in ESD protection circuit and 1T-DRAMs [1-2]. Z^2-FET works by modifying the forward bias operation of PIN diode and fashioning electrostatic barriers with the help of front-gate voltage (V_{GF}) and back-gate voltage (V_{GB}). The blocking of carrier conduction is only favorable when their diffusion length (controlled by carrier lifetime) is of the order of channel length. Hence, in this work, we evaluate the dependence of Z^2-FET device operation on the vital parameter: Carrier lifetime.

II. Device Specification and Characterization

The Z^2-FET (Fig. 1) is fabricated with 28 nm FDSOI technology with ultrathin silicon film (T_{si} = 7 nm) and thin buried oxide (T_{BOX} = 25 nm). Raised epitaxial layer (T_{epi} = 15 nm) in anode, cathode and ungated regions reduces the series resistance. Gate length (L_g) and ungated length (L_{int}) of measured/simulated device are 200 nm. Fig. 2 shows typical hysteresis in measured I_A-V_A characteristics for various V_{GF}. Two different states ('1' and '0') correspond to high or low current levels. Width of hysteresis window increases with V_{GF} as a result of progressive shift of turn-on voltage (V_{on}) due to stronger injection barriers created by gates.

III. Role of Carrier Lifetime

A. Callibration of transient and DC simulations

Current-based DC simulations are performed with maximum carrier lifetime (τ_{max} in SRH doping dependent model [3]) values of 10^{-10} s, 10^{-9} s, 10^{-8} s and 10^{-7} s. For $\tau_{max} \leq 10^{-9}$ s, an S-shape curve (snapback) with negative resistance region is achieved (Fig. 3). However, for $\tau_{max} \geq 10^{-9}$ s simulation fails to converge. To test if the non-convergence is a limitation of numerical simulator due to an inappropriate lifetime values, initial very fast transient (10 ns) gate voltages were ramped, followed by a very slow transient (50 s) applied to anode to achieve more realistic approach as in measurements. It resulted in hysteresis which matched well the snapback achieved with the DC simulation for $\tau_{max} \leq 10^{-9}$ s (Fig. 3).

These simulations reveal that the time required for the charge under the gates to reach the steady state is a strong function of carrier lifetime. As shown in Fig. 4, the total charge under the gate after the application of gate pulses, stabilizes at ~ 200 ms for $\tau_{max} = 10^{-10}$ s and around 20 s for $\tau_{max} = 10^{-9}$ s. For $\tau_{max} = 10^{-7}$ s, even after hundreds of seconds, the charge keeps on increasing. Carrier generation is responsible for filling the deeply depleted wells created by the gate pulses. However, for $\tau_{max} = 10^{-7}$ s, it is not possible to saturate the wells and to reach equilibrium. Note that for this lifetime value, the DC simulations fail to converge. On the other hand, the time taken to perform DC measurements is around tens of seconds. It hints that the actual lifetime of Z^2-FET cannot be longer than 10^{-8} s.

B. Z^2-FET Operation

Based on the previous paragraph, τ_{max} appears to be within 10^{-8} and 10^{-10} s due to the presence of snapback. Z^2-FET operation can be suitably simulated and analyzed in details with τ_{max} in above mentioned range. For example, in Fig. 5, the characteristic is simulated with $\tau_{max} = 10^{-10}$ s. Three main regions of operation are identified: (1) OFF state, (2) exponential region and, (3) ON state. In OFF state, the electrostatic barriers created by both gates are maintained beyond the diode turn-on point (V_A>0.6V). As shown in Fig. 6, potential under the front gate significantly increases with V_A, whereas in the ungated region, the potential variation is limited (~ 0.1 V). At the end of OFF state regime, the potential under the gate reaches its maximum value albeit the hole injection barrier (body/P+ barrier) is lowered to 0.5 V. In exponential state (Fig. 7), the potential at ungated side and electron injection barrier (N+/body barrier) are significantly reduced which is being reflected by current increase with V_A. Current rises sharply at the steep transition point, turning the device ON.

Device behaves like ON state of a PIN diode, leading towards double injection [4]. Fig. 8 relates various potential barriers present in device with V_A. Increase in V_A is mostly endured by center barrier (ϕ_C), which keeps Z^2-FET blocked in OFF state (Fig. 9). Once ϕ_C collapses, the voltage available on the injection barriers is increased more than necessary for the device to turn ON. The current increases even if V_A is reduced, which explains the S-shape curves and hysteresis.

IV. Conclusion

The work indicates the pivotal role of carrier lifetime in the modeling of Z^2-FET and provides guidelines to correctly model and characterize the device. Operation of Z^2-FET is chiefly governed by carrier generation to refill the potential wells and by recombination mechanism during well emptying, during reverse scan and ON state. A relatively long lifetime impedes sharp switching capability owing to slow generation of carriers.

Acknowledgment

Financial support from EU project REMINDER is appreciated.

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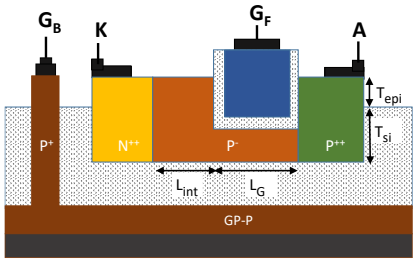

Figure 1. Schematic diagram of the measured/simulated device.

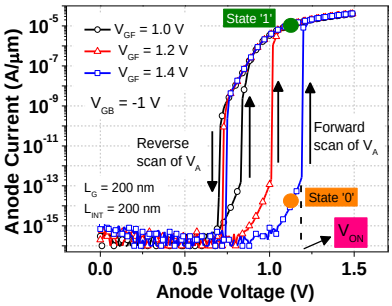

Figure 2. Experimental hysteresis in I_A-V_A curves of Z^2-FET for different V_{GF}.

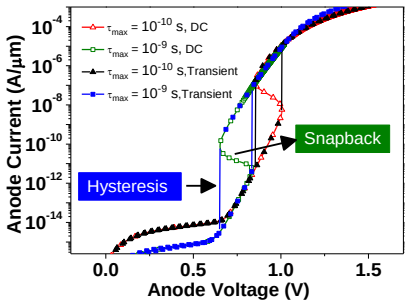

Figure 3. Correlation between DC and slow transient I_A-V_A characteristics for lifetime of 10^{-9} s and 10^{-10} s (simulation).

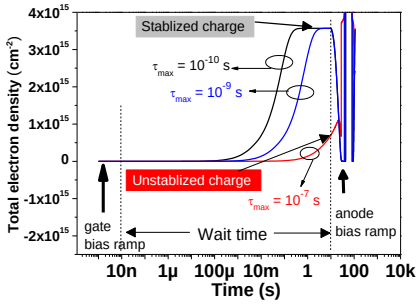

Figure 4. Integrated electron density under gate with lifetime of $\tau_{max} = 10^{-10}$ s, 10^{-9} s and 10^{-7} s (simulation).

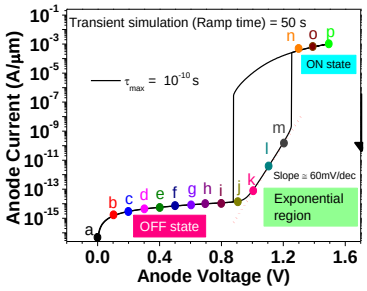

Figure 5. Three regions of operation of Z^2-FET as shown in I_A-V_A characteristics for $\tau_{max} = 10^{-10}$ s (transient simulation).

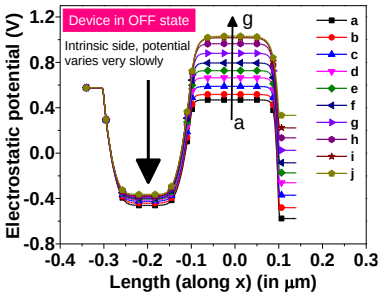

Figure 6. Electrostatic potential profile at the center of the device ($y = T_{si}/2$) during OFF state (simulation).

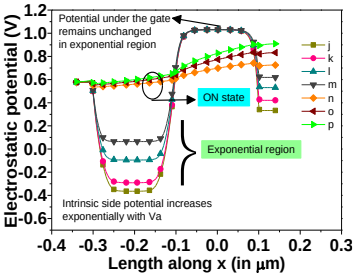

Figure 7. Electrostatic potential profile at the center of the device ($y = T_{si}/2$) during exponential and ON states.

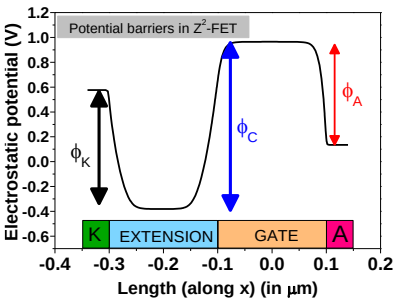

Figure 8. Different electrostatic barriers in Z^2-FET: ϕ_K, ϕ_A and ϕ_c.

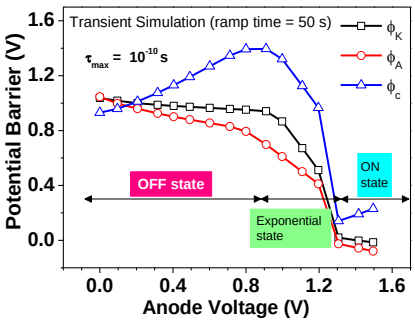

Figure 9. Dependence of different barriers in Z^2-FET on V_A.