Low temperature performance of proton irradiated strained SOI FinFET

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Abstract—This paper studies for the first time the low temperature characteristics of strained SOI FinFETs submitted to proton irradiation. Both types of transistors, nMOS and pMOS, were analyzed from room temperature down to 100K, focusing on the threshold voltage (VTH), subthreshold swing (SS), the Early voltage VEA and the intrinsic gain voltage (AV). The effects of strain techniques are also studied. The p-channel devices showed a greater immunity to radiation when looking at their digital parameters while nFinFETs had a better response to proton radiation from an analog parameters point of view.

Keywords—FinFET, low temperature, proton radiation, strained devices.

I. INTRODUCTION

The Silicon-on-Insulator (SOI) technology is well known for its superior performance in harsh environments, which includes radiation and high temperature. The fully depleted SOI (FD-SOI), which has a thin active silicon region, provides a better electrostatic coupling and the buried oxide located beneath the channel region accounts for its hardness against single event effects caused by radiation. However, the buried oxide located beneath the channel region accounts for the appearance of a parasitic conduction at the back interface that in turns degrades the SS values of n-channel transistors. However, when the focus is on p-channel devices, this shift towards a more negative VGS, turns off the parasitic conduction, which enhances the transistor off current [2, 3].

Focusing on the temperature influence, for unstrained nFinFETs, the reduction of SS is almost linear with temperature lowering as expected [4], however, it is not so linear for strained nFinFETs neither for p-channel devices. In these cases, both the effect of high interface trap density (Nt) and the VTn variation have to be taken into account as well. For strained FinFETs, where a higher Nt is observed [5], a non linear reduction of SS is obtained mainly due to the lower impact of Nt at low temperatures. This non-linear dependence with temperature is more pronounced for irradiated devices since the irradiation also promotes an increase of Nt. For p-channel devices, the parasitic conduction at the back interface is reduced due to not only the radiation effect as explained before, but the VTn variation with temperature reduction also contributes to it. The VTn increase at 100K is enough to suppress the back conduction for unstrained devices before radiation.

Analyzing the Early voltage (VEA) on figures 5 and 6, it is possible to notice that the values are kept almost constant as temperature decreases. A possible explanation is the competition between two mechanisms at low temperatures: the increment of the impact ionization rate that degrades VEA and the higher drain current level due to a higher carrier mobility, which tends to improve the value of VEA. Thus, these two mechanisms could keep the Early voltage at balance over the studied temperature range.

Looking at the intrinsic voltage gain (AV) (figures 7 and 8), it can be noticed that as the temperature changes, the AV values are slightly affected, even for irradiated devices. It can be explained by the fact that low temperatures although increasing the drain current (ID) and transconductance (gm) through some mechanisms — like better carrier mobility for example [4]— result in only a small gm/ID rate variation. Since the intrinsic gain voltage can be described as AV=gm/ID x VEA, the AV keeps the same VEA tendency. It is noticed for both nFinFETs and pFinFETs. For p-channel devices, the proton radiation causes a greater impact on the AV, being more pronounced on strained devices than on unstrained ones.

In summary, the pFinFETs have a better performance when looking at digital parameters VTH and SS after irradiation, mainly due to the negative shift of VTn caused by the charge buildup in the BOX. However, nFinFETs showed more immunity to proton radiation when analyzed from their analog parameter AV with a more stable response to temperature.

II. DEVICE CHARACTERISTICS

The devices evaluated in this study are multiple gate SOI MOSFETs (FinFETs), fabricated at imec, Belgium, on SOI substrates with a 150 nm thick SiO2 layer (BOX). The studied channel lengths Lc are 150 nm and 900 nm and three different fin widths Wf were compared: 20, 120 and 370 nm, with five fins in parallel. The gate dielectric consists of a 2 nm HfSiON layer on a 1 nm SiO2 interfacial layer, resulting in a 1.5 nm Equivalent Oxide Thickness (EOT). The gate is composed of a 10 nm thick TiN layer capped with 100 nm thick poly-Si. For all devices, the fin height Hf is 65 nm and the source and drain regions employ the Selective Epitaxial Growth (SEG) technique for reducing series resistance.

The irradiation process was performed at the Cyclone facility in Louvain-la-Neuve (Belgium). The proton radiation uses a 60 MeV beam energy, with a fluence of 1012 p/cm2 at normal incidence at room temperature. No bias was applied during irradiation and the contacts were kept floating.

III. RESULTS AND DISCUSSION

First, one of the main device characteristics, the threshold voltage (VTH), is analyzed (figures 1 and 2). For both n- and p-type FinFETs, it can be noticed that when the temperature decreases, the absolute VTH value increases, in an almost linear relationship, due to the increase of the Fermi level potential. The proton radiation affects in different ways the n-channel and p-channel devices. For the nMOS ones, the proton irradiation induces a negative shift of the VTH, what can be explained by the positive charge buildup in the front and buried oxide. This negative VTH shift in the Si/BOX interface results in an early parasitic conduction at the back interface. Even though this charge buildup also occurs for pMOS devices, the positive charges make the VTH more negative which turns off the parasitic back interface conduction in this case [2].

From figures 3 and 4, it can be noticed that narrow fin devices with short channels are less affected by proton irradiation when SS is analyzed. The wider or/and longer FinFETs exhibit a higher degradation of the SS parameter, due to a greater buried oxide area, which accounts for a larger charge buildup induced by radiation. This charge is responsible for the appearance of a parasitic conduction at the back interface that in turns degrades the SS values of n-channel transistors. However, when the focus is on p-channel devices, this shift towards a more negative VGS, turns off the parasitic conduction, which enhances the transistor off current [2, 3].

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In summary, the pFinFETs have a better performance when looking at digital parameters VTH and SS after irradiation, mainly due to the negative shift of VTn caused by the charge buildup in the BOX. However, nFinFETs showed more immunity to proton radiation when analyzed from their analog parameter AV with a more stable response to temperature.

CONCLUSIONS

The SOI FinFET devices were evaluated from four main points of view: operation temperature, radiation, fin width and strain, for both n-channel and p-channel devices. Narrow fin devices performed better in an overall analysis, with high values and low variation with temperature for the studied parameters and a higher immunity to proton radiation for digital parameters. The influence of both temperature and radiation is more noticeable on wide devices, mainly on the strained ones, where the effects of traps turned to be more significant.

Although focusing on digital parameters pFinFETs presented higher radiation hardness, nFinFETs had a better response for analog ones.
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The MSET Transistor as IC Building-Block

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Abstract—The Multistate Electrostatically Formed Nanowire Transistor (MSET) features a multigate structure, compatible with SOI fabrication process. The MSET enables the implementation of various fundamental analog and digital functions with a reduced number of components compared, e.g., with CMOS technology. Due to its low off-current, the MSET is ideally suited for low-power IoT applications operating at moderate frequencies. We present the MSET’s general structure and show several analog and digital consequential building blocks for integrated circuits.

Keywords—Multigate Transistor, Nanowire Transistor, Analog functions, Low Power Device

I. INTRODUCTION

The integration of nano-sensors into Internet of Things (IoT) platforms is likely to increase drastically in the near future. The incorporation of these sensors into IoT applications entails practical, fabrication-efficient and low-power solutions for their co-integration with circuitry supporting the sensors’ data flow. The tunable-diameter electrostatically formed nanowire (EFN) developed in our research group, has recently been demonstrated as a robust gas and temperature sensor [1]. Based on the EFN fabrication process, we then introduced a novel multigate transistor, called the MSET (Multiple-State Electrostatically Formed Nanowire). The MSET transistor can be fully compatible with SOI processes, and furthermore, paves the way for a monolithic IoT platform.

A schematic illustration of an MSET is shown in Fig.1, accompanied by a top-view of the device with its characteristic dimensions specified. The MSET comprises an N-type bulk ($N_d = 5 \cdot 10^{17} \text{cm}^{-3}$), a heavily doped source electrode ($N_d = 1 \cdot 10^{20} \text{cm}^{-3}$), two drain electrodes ($N_d = 1 \cdot 10^{19} \text{cm}^{-3}$), denoted D1 and D2, and heavily doped side-gates ($N_a = 1 \cdot 10^{19} \text{cm}^{-3}$) on each side of the bulk, denoted SG1, SG2. The device shall be denoted ‘N-MSET’ or ‘P-MSET’ Depending on the type of dopants in the bulk (either P or N). Correspondingly, the side gates are to be doped with the opposite type of dopants. To extend the MSET utility further, top or bottom gates can be placed above or below the bulk [2], respectively.

Figure 1. Left: Illustration of the two-drain MSET. Right: MSET top-view with dimension specified. Bottom: MSET – Block representation

II. PRINCIPLE OF OPERATION

In the N-MSET device depicted in Fig.1, each side-gate forms a P+N junction with the adjacent bulk. Voltage difference is set between the Source and both drains terminals. When both side gates are zero or negatively biased, the bulk is being fully depleted of free charge carriers, hence inducing a very high impedance between the drains-to-source terminals. When either side gate is positively biased, the potential barrier in the bulk space near the respective side-gate drops, and a conduction channel surrounded by depletion regions is formed on the path from the source to the drain (closer to the positively-biased side gate). Most importantly, the lateral position of the conduction channel from source to either D1 or D2 is controlled by applying asymmetrical or differential bias between the coupled side gates. Altering the lateral conduction path from S to either $D_{1,2}$ also determines the path’s impedance value, thus allowing the implementation of analog and digital functions, as demonstrated in the following section.
III. MSET-BASED ANALOG/DIGITAL FUNCTIONS

While originally envisioned as a stand-alone switch that can multiplex the data flow from the drains [3] into the source, miniaturization of the original MSET prototype to the dimensions specified in Fig.1, as well as reduction of its supply voltages, has prompted the realization of a rather diverse family of analog and logical functions. Owing to the ability to cascade two or more MSET transistors, the function realized by the MSETs is determined by their specific connection topology.

As an example, Fig.2 depicts a simple amplifier, involving two MSETs in a complementary arrangement (N-MSET and P-MSET on the left-hand and right-hand sides, respectively). When SG1 (connected to $V_{in}$) is biased HIGH (+0.25V), the conduction path from $S \rightarrow D_1$ in the P-MSET is being cut-off due to the high potential barrier for holes at the SG1-to-Bulk interface region. In the N-MSET On the other hand, the HIGH SG1 input facilitates the current flow from $S \rightarrow D_1$. Therefore, the voltage divider formed between the two complementary MSETs inverts the output with respect to the HIGH input, yielding LOW output ($V_{ss} = -0.25V$) at D1. The LOW output at D1 is then fed into the second side-gate SG2, causing the opposite complementary behavior to occur at the $S \rightarrow D_2$ path of the two MSETs. As a result, the input signal in $V_{in}$ is inverted twice, yielding a HIGH output at D2 ($V_{out} = V_{dd} = 0.25V$). The voltage gain in D2 is doubled with respect to that of D1, ensuring an overall steep voltage gain as seen on Fig.2 (Right). Moreover, by introducing the MSETs with an additional top gate, the steep LOW-to-HIGH transition point in Fig.2 could be modulated across the $V_{in}$ axis, paving the way for developing an MSET-based voltage comparators to serve A/D architectures in later stages.

In this amplifier and throughout all other MSET applications, the supply voltages ($V_{dd}, V_{ss}$) and the I/O dynamic voltage range are maintained at [-0.25V, 0.25V] to prevent excess forward current between the terminal electrodes and the SG-to-bulk junctions. The potential to use a supply voltage below 0.5V can offer significant power dissipation savings.

Schematics for an MSET-based NAND, NOR and a volatile memory cell are depicted in Fig.3. In keeping with the MSET block representation on Fig.1, the ‘N’ and ‘P’ labels in Fig.3 denote an N-MSET and a P-MSET transistors, respectively. It should be noted that computation of the MSET NAND and the NOR functions require roughly one half the number of MSETs as transistors requires by, e.g., CMOS technology. Similar to the MSET amplifier described above, the NAND/NOR operation is based on the formation of an impedance mismatch between the N- and the P-MSET transistors in the complementary structure, so as to induce either high $V_{dd} = +0.25V$ or low $V_{ss} = -0.25V$ output in $V_{out}$. Simulations pertaining to these logic gates (TCAD-Sentaurus) exhibit negligible static power consumption.
in the order of \( nW \), whereas transient simulations show the dynamic power consumption to be in the order of few \( \mu W \).

IV. CONCLUSIONS
The conceptually novel set of analog and logic functions based on the SOI MSET transistor, offer a multi-purpose computing capabilities suited for IoT applications of ultralow-power and low off-currents. The multigate nature of the MSET permits an increased flexibility for the design of logic gates with reduced number of transistors.

REFERENCES
A virtual SOI diode with electrostatic doping

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Abstract—Highly reconfigurable FD-SOI diodes with electrostatic doping are presented. Experiments show that the virtual p-n junction with gate-induced doping exhibits more or less conventional diode characteristics. A clear advantage of the virtual diode is that the doping levels are adjustable by the front and back gate biases. This flexibility enables the tuning of reverse current, forward current and breakdown voltage. Measurements and simulations explain why the models developed for standard diodes with physical doping do not apply.

Keywords—Silicon-on-insulator (SOI); p-n diode; virtual doping; electrostatic doping.

I. INTRODUCTION

The ‘electrostatic’ doping is a unique feature of Fully-Depleted Silicon-On-Insulator (FD-SOI) technology. In an ultrathin SOI device, a positive gate bias induces a quasi-uniform electron population in the entire film. The undoped body thus behaves as an N-type region and, for negative bias, as a P-type region. This doping metamorphosis has been used to conceive various devices such as TFET [1], Z²-FET [2], GDNMOS [3], I-MOS [4], etc.

The question is whether a virtual p-n junction can behave as a physical p-n diode. Previous studies have demonstrated the feasibility of electrostatic diodes, so called Charge Plasma p-n diodes [5, 6], using metal layer deposition with two different work-functions able to induce electrostatically P and N regions with rather constant doping. We are advancing this concept by proposing a diode where doping levels are adjustable by the biases of the front and back gates. Our device is a PIN diode with extended gate underlap and undoped body (Fig. 1, [1, 2]). Negative bias on the gate induces a virtual P⁺ region that extends the anode P⁺ contact. Similarly, positive bias on the back gate emulates the N⁺ region that extends the cathode N⁺ contact. We investigate the properties of the virtual P⁺-N⁺ diode.

II. DEVICE FABRICATION AND EXPERIMENT

Test devices were fabricated with state-of-the-art FD-SOI technology. The thicknesses of Si film and buried oxide (BOX) are tfilm = 7 nm and tbox = 25 nm. The BOX separates the undoped film (residual doping N_A = 10¹⁵ cm⁻³) from a highly doped P-type ground plane (N_A = 10¹⁸ cm⁻³) acting as a back-gate. To reduce series resistance, in situ Si epitaxy was performed on the highly doped N and P terminals (~10²⁰ cm⁻³). The equivalent oxide thickness of high-k/metal-gate stack is 3.7 nm. We consider relatively long diodes with equal length of gated and ungated regions (L_g = L_u = 500 nm). The reverse and forward currents of virtual diodes were measured for different combinations of gate and ground-plane biases at room temperature.

![Figure 1. Schematic of fabricated virtual diode. P⁺ and N⁺ doping is induced by front and back gate biases.](image)

III. EXPERIMENTAL RESULTS

The characteristics of electrostatic diodes (Figs. 2-5) look alike those of conventional diodes with physical doping. However, a detailed analysis points on significant differences.

![Figure 2. Experimental I-V characteristics of the virtual diode for two different doping levels. (1): V GF = -1.2 V, V GB = 5 V. (2): V GF = -2 V, V GB = 15 V. The reverse current is in absolute value. L_g = L_u = 500 nm, width = 1 µm, T = 300 K.](image)

**Reverse Current.** For relatively low anode reverse bias V_R, the current stays constant and extremely small (10⁻⁸ µA/µm) as long as P-doping is maintained. The ON/OFF ratio reaches 10¹⁰. A sudden increase in reverse current is observed when the gated body becomes fully depleted (see Fig. 3a). Not only massive carrier generation occurs
under the gate but also the P’ doping level vanishes exponentially in subthreshold region. For higher back-gate bias (Fig. 3b), the virtual P’-type doping and corresponding low-leakage region subsist only for highly negative top gate voltage $V_{G}$. Numerical TCAD simulations show the contributions of generation, diffusion and tunneling mechanism according to the level of electrostatic doping.

**Forward Current.** The forward I-V curves in Fig. 4 again look familiar [7]. At low bias, the recombination current prevails and follows $I \sim e^{V/2kT}$. The diffusion current $I \sim e^{qV/kT}$ dominates at higher voltage. These currents depend on the concentration of electrostatic doping. The ideality factor $n$, calculated from $I = I_0 \exp (qV/kT)$, is shown in Fig. 5. The transition from recombination to diffusion current is indicated by the inflection point $T$ and it occurs at $\sim 0.8$ V. At even higher voltage (> 1 V), the ideality coefficient degrades due to high injection and series resistance effects.

Figure 3. Reverse current-voltage characteristics of the virtual diode measured with variable front-gate bias: (a) $V_{cm} = 5$ V, (b) $V_{cm} = 10$ V. Parameters as in Fig. 2.

Figure 4. Forward current-voltage characteristics of the virtual diode measured for variable bias on front and back gates. Parameters as in Fig. 2.

Figure 5. Ideality factor extracted from Fig. 4 versus forward voltage. Point $T$ indicates the transition from recombination current to diffusion current.

**Typical features.** Unlike physical diodes, the virtual diode does not maintain symmetrical characteristics when biasing the anode or the cathode. The doping level changes dynamically with diode bias, for example P’ concentration increases as $V_A$ becomes more positive. Carrier generation/recombination is not limited within the junction but can occur in all regions that eventually become fully depleted. The reverse current and breakdown voltage are fully tunable with the gates.

**IV. CONCLUSION**

We have demonstrated an astonishing SOI diode with virtual doping. The doping level is manipulated by the front and back gate biases. This flexibility is attractive for matching user-defined applications. Although our experimental results show typical ‘diode-like’ characteristics, the virtual diode cannot be modeled with the conventional p-n junction theory. We argue that the combination of the lateral junction field with the vertical gate-induced field implies a 2D description.

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MOSFETs in the VeSTIC process - fabrication and characterization

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Abstract—A method for extraction of physical parameters of the transistors in the VeSTIC technology is proposed. The flat-band voltage, mobility and radius of the slit curvature are extracted from the I-V characteristics of a single VeSFET. The method has been presented based on experimental devices manufactured in ITE.

Keywords—VeSTIC, VeSFET, CMOS technology, electrical characterization

I. INTRODUCTION

A VeSTIC technology has been proposed in [1, 2] as a competitor for FinFETs for the sub-22nm technology nodes. The devices in the VeSTIC integrated circuits are designed based on regular arrays of circles, which are the elementary shapes in the design. Such ICs should be resistant to the patterning distortions. The technology is designed for manufacturing of the CMOS devices, called VeSFETs. However, manufacturing of BJTs with polysilicon emitters and collectors, or JFETs with polysilicon gates is also possible. Moreover, different types of devices can be fabricated in parallel. The VeSFETs can be designed with tied or independent gates. The electrical measurements have revealed the promising I-V characteristics of the VeSFETs with a high \( I_{on}/I_{off} \) ratio of the order of 10\(^7\) and a good subthreshold slope as low as 65 mV/dec [2, 3]. Such features of this technology enable e.g., low-power IC fabrication, or realization of single MOSFET logical gates [4]. Recently, the VeSFETs have been subject to the detailed analysis based on extensive numerical simulations [5].

The VeSTIC process design rules and the IC layout are determined by the radius \( r \) of the circle, which is the elementary patterning element. The radius as well as the doping concentration and carrier mobility in the VeSFET channel are of primary importance. A simple approach for identification of these parameters is proposed in the presented work.

II. DEVICE FABRICATION

The experimental test devices have been manufactured in ITE using the VeSTIC process. They are arranged as 4x4 arrays of transistors differing with the slit projected radius. Each pad is shared by two neighboring devices. This design is not consistent with the original VeSTIC concept, where both the device channels and the electrodes are patterned using identical circular shapes. In our case only the circular shape of the silicon slits is preserved. The pads (much larger than the active areas) are rectangular, whereas the access regions between the slits and the pads are triangular. The devices in the modules differ also with the slit width, which is defined by photolithography, not by the radius \( r \) only. In Fig.1 a part of the test structure layout is shown, highlighting the details of the VeSFET module. The devices have been manufactured using the 4-inch SOI wafers. They have channels 170 nm high with \( 3.6 \times 10^{17} \) cm\(^{-3} \) doping concentration. Two types of the patterning have been used, namely the standard projection photolithography and the electron beam lithography (EBL). The slits have been finally formed by the plasma etching process. A part of the fabricated test structure with the VeSFET module is shown in Fig.2. The VeSFETs with different curvatures of the channel are shown in Fig.3.

![Figure 1. The layout of the VeSFET test module; in the inset a single transistor is shown in detail](image)

III. CHARACTERIZATION METHOD

The proposed characterization method is based on the VeSFET compact model [6]. It may be used for characterization of the slit based on the VeSFET I-V characteristics. Our work regards devices with the tied gates. At the depletion below the gate and for non-satu-
One can easily recognize the first term in (4) as the current at the flat band conditions $I_{D,fb}$, and the second one as the transconductance $g_m$. Using the linear fit based on:

\[(I_D)^2 g_m V_{GS})(V_{DS}) = I_{D,fb}/V_{DS} - V_{DS}^2 g_m /V_{DS} \] (5)

resulting from (4) the $V_{fb}$ may be directly extracted. Additionally, if the channel doping is known, then the mobility may be estimated as well. Next, using the linear regression (4) the channel length $L$, thus the slit radius $r$ may be estimated.

IV. DEVICE CHARACTERIZATION

The I-V characteristics of the n-channel VeSFET have been measured. The threshold voltage is 0.86 V, the subthreshold slope is 88 mV/dec. The $I_d/I_{sat}$ ratio is of the order of 10$^6$, so it may be stated that the device under test exhibits a satisfactory behavior. Based on these $I_d$-$V_{GS}$ data the following parameter values have been calculated: $V_{fb}$=1.77 V, $\mu$=108 cm$^2$/Vs, $r$=380 nm (Fig.4). The rather low mobility value is probably due to the significant carrier scattering induced by the rough Si-SiO$_2$ interface resulting from plasma etching of the silicon slits. The radius value is close to the expected one, what is also confirmed by SEM observations.

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