Silicon tunnel FET with average subthreshold slope of 55mV/dec at low drain currents

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***Abstract*— In this paper we present a silicon tunnel FET based on line-tunneling and reduced trap-assisted tunneling(TAT) to achieve better subthreshold performance. The device achieves an I_{on}/I_{off} ratio of 10^6 and average SS of 55mV/dec over two orders of magnitude of I_d. Furthermore, the analog figures of merit have been calculated and it is shown that transconductance efficiency g_m/I_d beats MOSFET performance at lower currents.**

Keywords- steep-slope device; tunnel FET; line-tunneling, trap-asissted tunneling;

I. INTRODUCTION

Tunneling FETs are promising candidates to overcome MOSFETs subthreshold slope (SS) limit of 60 mV/dec for low power computing and internet of things applications. Unlike MOSFETs which rely on thermionic emission of electrons over a barrier, TFETs exploit quantum mechanical band to band tunneling of carriers from source to channel. This effect has little dependence on temperature and also filters out high and low energy tails of the Fermi distribution of carriers leading to steeper switching slopes [1]. Experimental demonstrations of TFETs using different materials have been already been reported [2],[3]. Among these materials Si TFETs show the best I_{on}/I_{off} ratio [4], However, Si TFETs still suffer from degraded SS due to trap assisted tunneling (TAT) caused by residual defects induced by ion implantation and high-k interface defects.

In this paper, we present a novel approach to decrease TAT and take advantage of line tunneling with source-gate overlap. It has been shown that line-tunneling can lead to steeper subthreshold slopes with respect to point tunneling. [7] We accomplish this by first implantation and thermal activation and then etching down the source area to remove the end of range (EOR) implantation damage. Moreover, to promote line-tunneling there is an overlapping source-gate area over the thin source region.

II. DEVICE FABRICATION

The devices were fabricated on a 20nm SOI wafer as starting substrate. First, PECVD SiO_2 was deposited and patterned to form the dummy gate. Then tilted implantation of boron and phosphorous ions followed by high temperature spike annealing at 1050 °C was carried out. Subsequently the dummy gate was removed and 60nm PECVD SiO_2 was deposited and patterned to open a window for thinning down the source junction. The source was etched down to 5nm at room temperature in a solution of TMAH and IPA for 2 minutes. Afterwards, 3nm of ALD HfO_2 and 60nm of PVD TiN were deposited and patterned to form the high-k/MG stack. Figure 1 schematically summarizes important process steps. 2nm of Ni were deposited and annealed to form $NiSi_2$ as contacts.

III. RESULTS AND DISCUSSION

Figure 2 presents the I_d-V_g transfer characteristics of the fabricated pTFET device with 2µm channel length and 2µm gate width. A high I_{on}/I_{off} ratio of 10^6 at V_d = -0.1V and an average SS of 55mV/dec over two orders of magnitude from $I_d = 10^{-13}$ to $I_d = 10^{-11}$A/µm is achieved, which is very promising for silicon TFETs. By increasing V_d the ambipolar current increases which in turn leads to SS degradation. It is worth noting that all the points used for calculating SS have been at least one order of magnitude larger than gate leakage. Figure 3 shows the calculated SS for each point of the transfer characteristics. Apparently, SS decreases below 60mV/dec for several points with a minimum of 30mV/dec but degrades by increasing I_d which is the expected behavior of TFETs due to non-ideal junction sharpness. Figure 4 shows output characteristics with the current density of 0.4 µA/µm at $V_d = V_{OV}$ = -0.5. Here V_{ov} is calculated by taking corresponding V_g to $I_d = 10^9$ A/µm as V_T. Output Characteristics also shows good saturation of I_d and typical super linear onset.

To investigate the analogue performance of this device, g_m/I_d and g_d have also been calculated as shown in Figure 5 and Figure 6. The transconductance $g_m = \partial I_d/\partial V_g$ is a measure of the electrostatic gate control. g_m/I_d is the transconductance efficiency and is an important analog device figure of merit as it relates current consumption to amplification performance. As shown in Figure 5, g_m/Id surpasses the MOSFET limit and reaches the maximum value of 55 1/V. Figure 6 depicts that output conductance g_d tends to small values which indicates good saturation of I_{on} and good intrinsic gain of the pTFET.

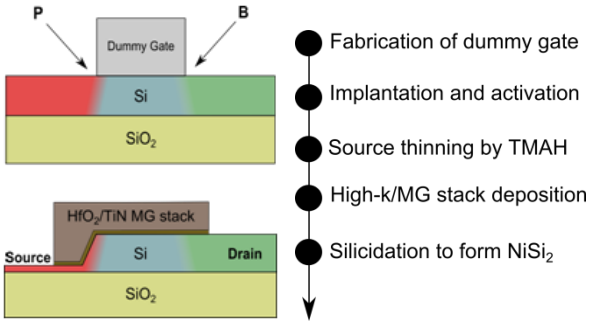

Figure 1. Schematics and important fabrication steps

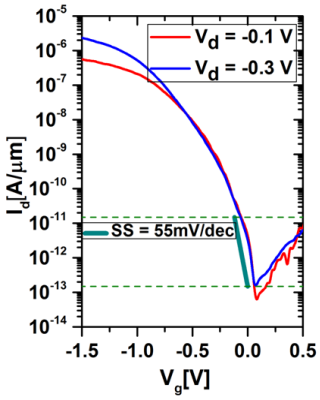

Figure 2. I_d-V_g Transfer characteristics of the pTFET.

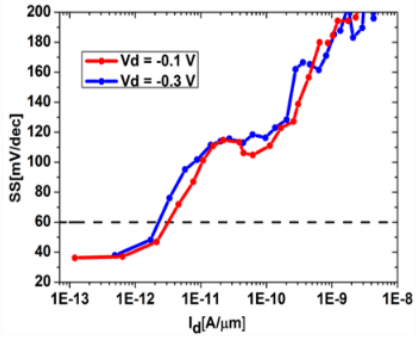

Figure 3. point SS vs I_d

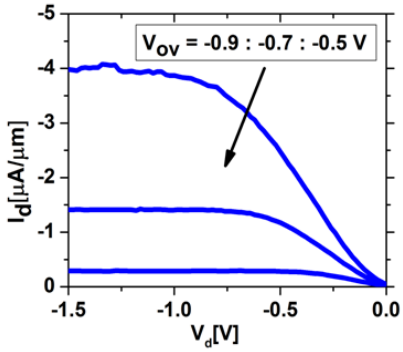

Figure 4. Output characteristics I_d-V_d

IV. Conclusion

We have fabricated Si p-TFETs with improved SS due to a reduction of TAT achieved by removing the EOR damages from implantation with a wet etch process.

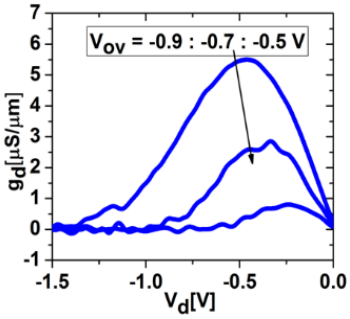

Figure 5. output conductance g_d

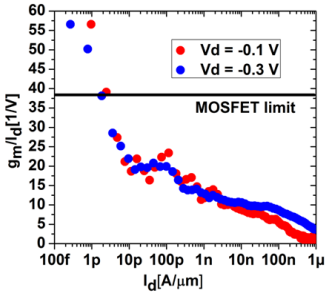

Figure 6. g_m/I_d transconductance efficiency vs I_d

Moreover, an overlap of source and gate area gives rise to line tunneling which further enhances the subthreshold slope. An average SS of 55mV/dec over two orders of magnitude of I_D was achieved.

Acknowledgment

This work is partially supported by the BMBF project UltraLowPow (16ES0060K) and the European project E2SWITCH.

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Performance and Transport Analysis of Vertically Stacked p-FET SOI Nanowires

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1. Abstract

This work presents the performance and transport characteristics of vertically stacked p-MOSFET SOI nanowires (NWs) with inner spacers and epitaxial growth of SiGe raised source/drain. Electrical characteristics are shown for [110] and [100] channel orientations, as a function of both fin width (W_{FIN}) and channel length (L). Results show a good electrostatic control and reduced short channel effects (SCE) down to 15nm gate length. Improved effective mobility is obtained for [110]-NWs due to higher sidewall mobility contribution.

2. Introduction

Nanowires MOSFETs have shown to be a good alternative to FinFET technology for the continuity of the CMOS roadmap due to great performance and scalability [1] [2]. Higher electrostatic coupling is the responsible for triple gate (3G) and Gate-All-Around (GAA) NWs outperforming short channel FinFETs [3]. To fulfill higher drive current requests, the performance of multiple gate structures [4] have been improved thanks to mechanical stress and rotated substrates. While the use of compressive stress and tensile stress can enhance holes and electrons mobility respectively [5], [100]-orientated NWs can boost electrons mobility due to higher mobility along (100) sidewalls [6].

Recently, vertically stacked NWs have been successfully fabricated due to advanced process developments. They combine reduced SCE and improved on-state current (I_{ON}) due to higher device aspect ratio, as the overall channel width (W_{eff}) [7-9] is increased. In this work we present, the performance and transport of vertically stacked p-FET SOI NWs fabricated with inner spacers and SiGe raised source/drain [9]. The analysis is performed as a function of both W_{FIN} and L, for NWs orientated along [110] and [100] directions. The I_{ON}/I_{OFF} behavior, gate-to-channel capacitance (C_{GC}), threshold voltage (V_{TH}) roll-off, subthreshold slope (S), DIBL, series resistance (R_S) and effective mobility (μ_{eff}) are evaluated and discussed.

3. Devices and Measurements

Vertically stacked NWs with two levels of NWs have been fabricated at CEA-LETI, starting from SOI wafers with 145nm BOX thickness and using a replacement metal gate (RMG) process. Fig.1 shows TEM images of the cross section and the longitudinal section of the stacked-NWs MOSFET. The wire at the bottom presents a Ω-shaped gate while the wire at the top is GAA. Both levels have a 10nm thick Si channel. Further fabrication details of stacked-NWs MOSFETs can be found in [9]. The gate stack is composed by a HfO_2/TiN/W. $Si_{0.7}Ge_{0.3}$:B raised S/D have been used in order to induce a compressive strain of up to 1% in both top and bottom channels. NWs have been fabricated along two crystallographic orientations, [110] and [100].

Fig. 2 presents C_{GC} measurements as a function of V_{GS} and W_{FIN} for [110]- and [100]-NWs and L=100nm. An EOT of ~1.2nm was extracted for both transport orientations by fitting the experimental C-V curves to those resulting from a Poisson-Schrödinger solver accounting for quantum confinement effects. The linear behavior of C_{GC} with W_{FIN}, extracted at the same gate voltage overdrive ($V_{GT}=V_{GS}-V_{TH}=-1V$), allows to conclude that the EOT is sustained with W_{FIN} scaling and channel orientation, indicating uniform and well controlled gate stack deposition process.

4. Results and Discussion

Fig. 3 presents the normalized drain current ($I_{DS}\times L$) as a function of the gate voltage (V_{GS}) for [110] (0°) and [100] (45°) NWs in multiple finger structures (50 fins), with L=30nm and 100nm, and $V_{DS}=-40mV$ and -0.9V. Higher drain current is observed in [110]-NWs, as expected for p-FETs. Indeed, hole mobility is enhanced in the (110)-oriented sidewalls in comparison to (100) plan. Additionally, the effect of a uniaxial compressive stress (induced here by SiGe S/D) become detrimental in narrow p-NWs with [100]-oriented channel ($\pi_{L,NW}^{[100]}<0$, see Fig.5 in [10]), which degrades even more the hole mobility in those devices. On the other hand, no significant subthreshold characteristics degradation is observed in the logarithmic scaled curves. From Fig. 4 one can observe similar off state current (I_{OFF} extracted at $V_{GS}=0V$ and $V_{DS}=-0.9V$) for both channel directions and a I_{ON}/I_{OFF} ratio in the order of $\sim10^4$, higher for standard devices and increasing with W_{FIN} reduction.

Fig. 5 shows the V_{TH} behavior with W_{FIN} and L, extracted by the second derivative method, at $V_{DS}=-40mV$. Improvements for narrower NWs and very small V_{TH} roll-off (lower than 60mV) is observed while reducing L down to 15nm. Fig. 6 shows S and |DIBL| results as a function of W_{FIN} and L. A small subthreshold slope degradation is obtained with channel shortening. For [110]-NWs with $W_{FIN}=25nm$, S is lower than 88mV/dec down to L=15nm. Through both S and |DIBL|, it is observed approximately constant dependence with W_{FIN} for L=100nm and 60nm and reduced SCE for narrower NWs for L=30nm. Besides, both [110]- and [100]-NWs exhibit similar results. |DIBL| is lower than 100mV/V for [110]-oriented NWs with $W_{FIN}=25nm$ and L down to 15nm.

R_S and mobility values were extracted by Y-function method [12]. Fig. 7 shows good linearity between the total resistance

(R_T=V_{DS}/I_{DS}) and the inverse of the NW gain (β), being R_S around 140 and 360Ω.µm for [110] and [100]-NWs, respectively.

The hole mobility $\mu_{eff}(N_{inv})$ extracted by split-CV technique [11] for L=100nm and W_{FIN}=15nm is shown in Fig. 8. The maximum mobility is found equal to 63 and 32cm^2/V×s for standard and rotated NWs, respectively. The μ_{eff} ratio between both [110] and [100]-NWs is close to 2, which agrees with the I_{ON}/W_{eff} results obtained in Fig. 4. Fig. 9 presents μ_{eff} as a function of L extracted by Y-function method and W_{FIN} extracted by split-CV technique, for several NWs, at N_{INV}=0.8×10^{13}cm^{-2}. Standard NWs show strong μ_{eff} degradation for L<60nm while rotated NWs present a constant, but lower, mobility down to L=30nm. Besides, μ_{eff} shows improvements of up to 17% with W_{FIN} reduction for [110]-NWs, while [100]-NWs show constant behavior, which is agreement with triple gate MOSFETs results [13].

5. Conclusions

Two levels stacked NWs present high I_{ON}/W_{FIN} (up to 2500µA/µm for [110]-NWs), although smaller μ_{eff} is expected for stacked p-NWs in comparison to 3G MOSFETs due to stronger top surface (100) contribution. Despite complex S/D engineering, small R_S obtained for [110]-stacked NWs are comparable to advanced planar MOSFETs results. Excellent SCE control (small V_{TH}, S and DIBL degradations down to 15nm gate length) have been obtained for both [110] and [100]-oriented NWs due to good electrostatic coupling and channel control provided by the sum of Ω-Gate and GAA wires. On the same way as for 3G NWs, [110] orientation is better for p-type stacked NWs due to hole mobility improvements in (110)-oriented sidewalls.

Acknowledgements: To the French Public Authorities from NANO 2017 program, CNPq and FAPESP processes 2015/10491-7 and 2016/06301-0. This work is also partially funded by the SUPERAID7 (grant N° 688101) project.

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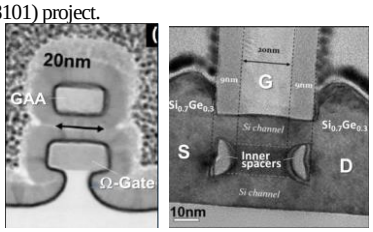

Fig.1: *Vertically stacked SOI NW cross section and longitudinal section TEM images.*

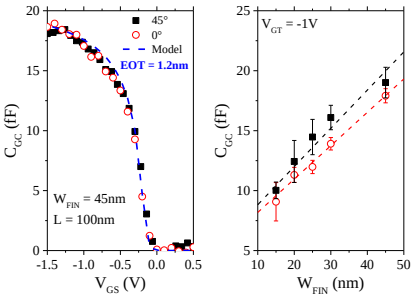

Fig.2: C_{GC} *vs* V_{GS} *and* W_{FIN} *for [110] and [100]-NWs, L=100nm.* C_{GC} *modelling allowed EOT extraction of 1.2nm.*

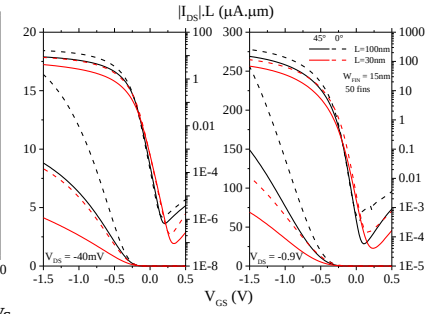

Fig.3: $|I_{DS}|\times L$ *vs* V_{GS} *for [110] and [100]-NWs, L=100 and 30nm, at* V_{DS}*=-40mV and -0.9V.*

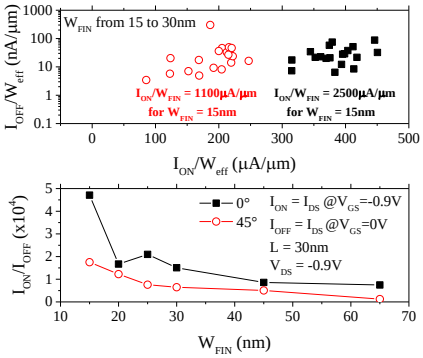

Fig.4: I_{ON}/I_{OFF} *characteristics for [110] and [100]-NWs with L=30nm, at* V_{DS}*=-0.9V.*

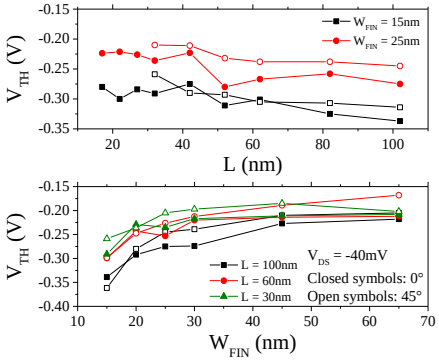

Fig.5: V_{TH} *vs L and* W_{FIN} *for several [110] and [100]-NWs, at* V_{DS}*=-40mV.*

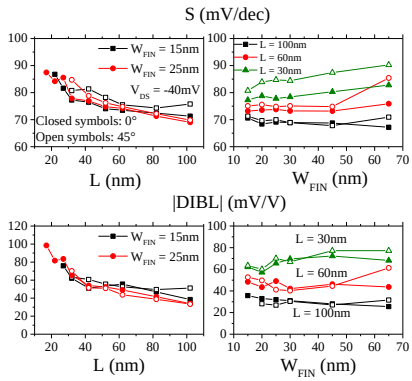

Fig.6: *S and |DIBL| vs L and* W_{FIN} *for several [110] and [100]-NWs, at* V_{DS}*=-40mV.*

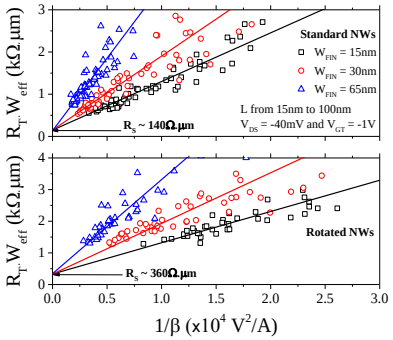

Fig.7: $R_T.W_{eff}$ *vs 1/β for several [110] and [100]-NWs.*

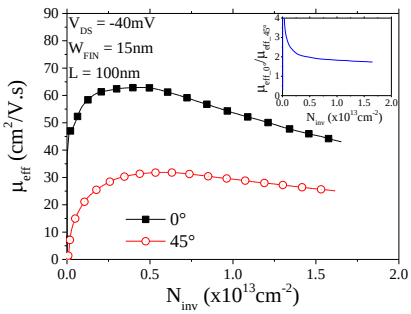

Fig.8: μ_{eff} *and* $\mu_{eff\_0°}/\mu_{eff\_45°}$ *vs* N_{inv} *for [110] and [100]-NWs, L=100nm and* W_{FIN}*=15nm, at* V_{DS}*=-40mV.*

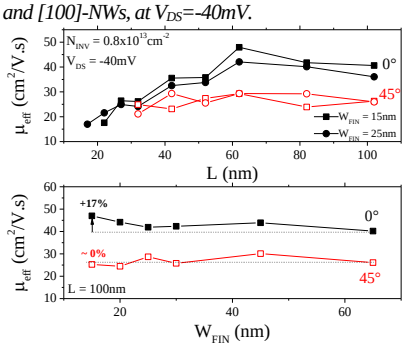

Fig.9: μ_{eff} *vs L and* W_{FIN} *for several [110] and [100]-NWs, at* N_{inv}*=0.8×10*^{13}*cm*$^{-2}$ *and* V_{DS}*=-40mV.*

Improved Analog Performance of SOI Nanowire nMOSFETs Self-Cascode through Back-Biasing

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***Abstract*—In this paper the analog performance of the Self-Cascode SOI Nanowire nMOSFET has been evaluated through experimental results, with regards to the variation of the channel width of the transistors near the source and the drain, and the back gate voltage.**

Keywords-Asymmetric Self-Cascode; Nanowire; analog performance; channel width; back gate voltage

I. INTRODUCTION

For the continuity of the CMOS roadmap, the transistors scaling is a mandatory appeal. In order to achieve better gate electrostatic control over the channel charges, multiple gate field effect transistors have been proposed, reducing short-channel effects and allowing transistors scaling [1]. The excellent performance of nanowires (NWs) for digital [2] and analog applications [3] has been already demonstrated. The self-cascode (SC) structure, shown in Fig. 1, is composed by two transistors in series association with gates shortened, and is an alternative to improve the analog characteristics of SOI MOSFETs [4]. In Fig. 1, W_S and W_D are the channel widths of the individual transistors near the source and the drain, respectively. Additionally, if the threshold voltage of transistor near the drain (M_D) is reduced in comparison with the transistor near the source (M_S), achieving the so-called asymmetric SC (A-SC), further improvements can be obtained in analog characteristics [5]. This paper intends to evaluate the analog performance of SC composed by nanowires. By changing the back-bias (V_{BS}), the threshold voltage can be modified, configuring an asymmetric self-cascode association, resulting in larger intrinsic voltage gain (A_V).

II. DEVICES CHARACTERISTICS AND RESULTS

The measured transistors are silicon triple gate SOI NWs fabricated at CEA-Leti [6], [7]. The devices present 145 nm thick buried oxide (BOX), gate stack composed by HfSiON/TiN (EOT=1.4nm), silicon thickness (H_{FIN}) around 11nm, channel length (L) of 100nm, and channel widths of 35 and 120nm, with 10 fins in parallel. Table 1 presents the extracted V_{TH} varying V_{BS}. From these results, it is possible to see higher influence of V_{BS} in V_{TH} for the wider transistor, which is linked to the poorer gate electrostatic control. The A-SC structure is composed by a transistor with larger V_{TH} near the source.

TABLE I. EXTRACTED THRESHOLD VOLTAGES.

NWs L=100nm	Threshold Voltage (V)		
	W=35nm	*W=120nm*	*SC W=35nm and W=120nm*
V_{BS}=-12V	0.47	0.50	0.48
V_{BS}=0V	0.43	0.37	0.41
V_{BS}=12V	0.37	0.17	0.35

This way, at V_{BS}=-12V, W=120nm is the M_S transistor and W=35nm is the M_D transistor. For the other values of V_{BS}, W_S=35nm and W_D=120nm. As expected, the increase of V_{BS} reduces V_{TH}, since there is a reduction of depletion charges controlled by the gate. In the case of the A-SC structure, V_{TH} tends to the threshold voltage of M_S transistor. Fig. 2 exhibits the drain current (I_D) and the transconductance (g_m) as a function of the gate voltage overdrive ($V_{GT}=V_{GS}-V_{TH}$) at V_{DS}=0.7V and V_{BS}=0V. One can verify that the A-SC present I_D and g_m similar as the single transistor (ST) with W_S=35nm, since M_S device is the dominant transistor [5]. Fig. 3 shows I_D and g_m against V_{GT} for the A-SC structure varying V_{BS}. It is possible to see that I_D and g_m are barely affected by V_{BS}, except for the larger g_m peak seen for V_{BS}=0V and 12V. In these cases, $W_D>W_S$, so the resistance of the M_D transistor is lower, increasing the intermediate potential between the M_S and M_D transistors (V_X in Fig. 1), and also g_m. By analyzing I_D, there is a similar subthreshold slope among the devices. This way, there is no degradation of electrical characteristics by applying V_{BS}. Besides that V_{BS}=-12V presents lower GIDL. Fig. 4 exhibits I_D and the output conductance (g_D) *versus* V_{DS} at V_{GT}=200mV and V_{BS}=0V for ST and A-SC. As one can note, the A-SC shows smaller I_D and g_D when compared with the ST, since part of V_D is absorbed by the M_D transistor, reducing V_X and its variation with V_{DS} [5]. In Fig. 5, it is presented I_D and g_D *vs.* V_{DS} for the A-SC at different V_{BS}. The larger V_{BS}, the lower g_D, since there is a larger V_{TH} gap between the M_S and M_D transistors [5]. Also, by using the wider transistor as the M_S, there is an increase of I_D and g_D since the M_S device is the dominant transistor, as observed before. Fig. 6 shows the Early voltage ($V_{EA}=I_D/g_D$) against V_{BS}. For ST, V_{EA} increased with nanowire narrowing. One can notice that the A-SC presents larger V_{EA} compared with ST, indicating that the reduction of I_D caused by the use of two transistors is less pronounced than the decrease of g_D. Besides that, a larger increase of V_{EA} is obtained at V_{BS}=12V. Fig. 7, 8 and 9

present g_m, g_D and $A_V=g_m/g_D$ as a function of V_{BS}. It is possible to observe that the change of V_{BS} does not affect significantly g_m, except for the W=120nm, which is related to the influence of back gate voltage in the control of channel charges. However, there is an important reduction of g_D with the increment of V_{BS} for the A-SC, since the V_{TH} difference increases, reducing channel length modulation effect. As previously mentioned, at V_{BS}=-12V, where $W_S>W_D$, g_D reduction is less significant in comparison to the SC where $W_D>W_S$ (reduction of 1.5 and 7.7 times, respectively). Since all A-SC presents lower g_D compared with ST, larger A_V is verified, mainly when V_{BS} is positive. Also, by reducing V_{GT}, there is a reduction of g_m and g_D, with the decrease of the latter being more pronounced, increasing A_V.

III. CONCLUSIONS

This paper studied the influence of back-bias on the analog performance of the self-cascode structures composed by nanowire transistors. It has been verified that the back bias promotes different V_{TH} variation between the devices. Larger V_{TH} gap between the M_S and M_D NWs allows an increase of A_V. Besides that, the association of a wider transistor near the drain and a narrow device near the source improves even more A_V.

ACKNOWLEDGMENT

This work was supported by FAPESP grant #2015/08616-6 and CNPQ grant #311408/2013-3.

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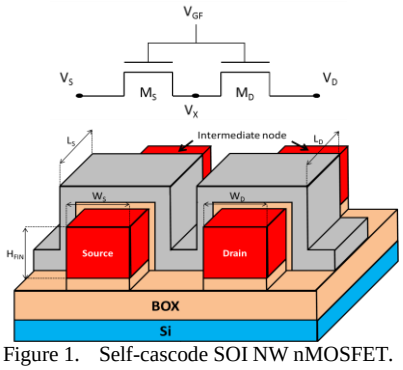

Figure 1. Self-cascode SOI NW nMOSFET.

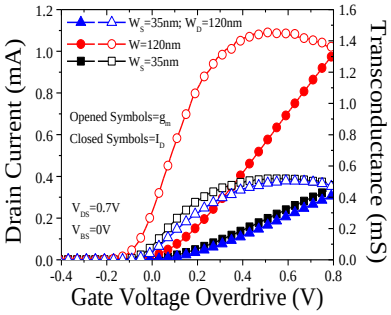

Figure 2. I_D and g_m as a function of V_{GT} at V_{DS}=0.7V and V_{BS}=0V.

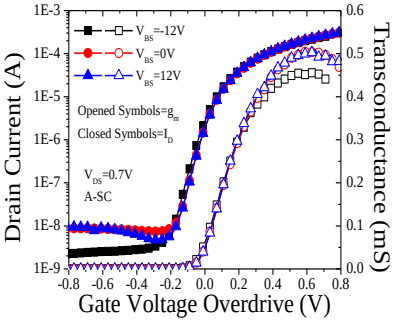

Figure 3. I_D and g_m as a function of V_{GT} for the A-SC at V_{DS}=0.7V.

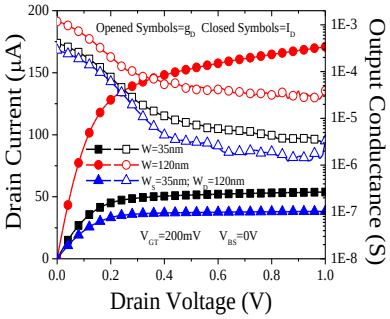

Figure 4. I_D and g_D as a function of V_{DS} at V_{GT}=200mV and V_{BS}=0V.

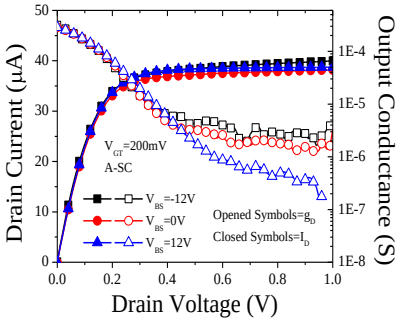

Figure 5. I_D and g_D as a function of V_{DS} for the A-SC at V_{GT}=200mV.

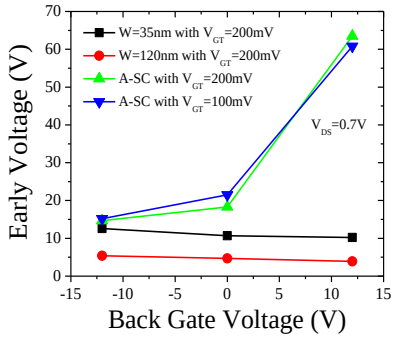

Figure 6. V_{EA} as a function of V_{BS} extracted at V_{DS}=0.7V and different V_{GT}.

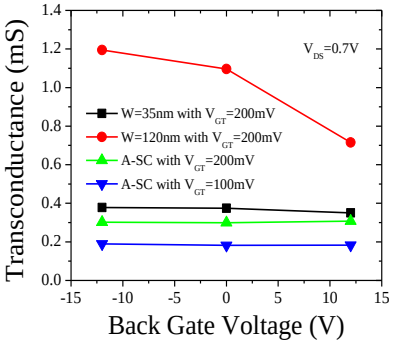

Figure 7. g_m as a function of V_{BS} extracted at V_{DS}=0.7V and different V_{GT}.

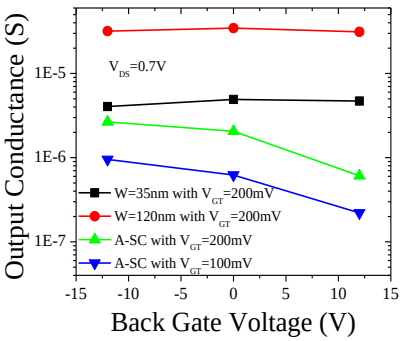

Figure 8. g_D as a function of V_{BS} extracted at V_{DS}=0.7V and different V_{GT}.

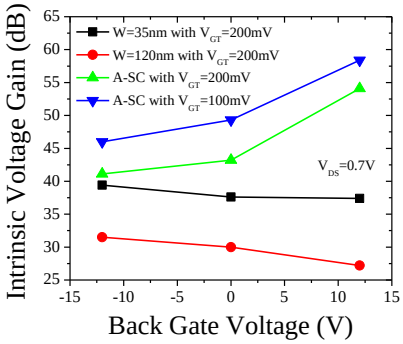

Figure 9. A_V as a function of V_{BS} extracted at V_{DS}=0.7V and different V_{GT}.

Dependence of MOSFETs threshold voltage variability on channel dimensions

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***Abstract*— The dependence of the MOSFET threshold voltage variability on device geometry (width (W) and length (L)) has been studied in detail from experimental data. Our results evidence, in agreement with other works, deviations from the Pelgrom's rule. In this work, a new empirical model has been proposed to reproduce more accurately the experimental data, considering that L and W have different influence on the device variability.**

Keywords-Pelgrom's law; charges; variability; MOSFET.

I. INTRODUCTION

Understanding the dependencies of the variability of the threshold voltage in MOS devices constitutes a challenge that must be faced in order to optimize the circuit design. According to Pelgrom's rule, MOSFET threshold voltage (V_{th}) variability is inversely proportional to the square root of the active transistor area [1]. However, significant deviations from this rule have been reported on experimental data, especially in 65 nm technologies and beyond [2], [3]. The possible causes of this deviation have been studied in previous works [4], [5], nevertheless, they have not been fully clarified yet. In this work, it is experimentally shown that the dependences of V_{th} variability associated to W and L should be decoupled. TCAD simulations have been performed in order to elucidate the physical origin of the different dependences. A simple empirical model that reproduces accurately the experimental data has been proposed.

II. RESULTS

A large set of pMOS and nMOS devices of different W and L manufactured in a 65 nm CMOS technology have been characterized. Table I indicates the number of DUTs tested for each device geometry. Note that in some cases W and L are fixed (yellow and green cells in Table I), which allows to study the V_{th} variability when only one of the dimensions is changed. The V_{th} of each device was obtained from the devices Id-Vg curves (V_D = 100 mV), by applying the constant current method.

	Device dimensions W/L (nm)							
DUTs	592	16	16	16	36	36	36	36
W	80	200	600	800	1000	1000	1000	1000
L	60	60	60	60	60	100	500	1000

Table I: Number of devices analyzed for each type (nMOS and pMOS) and W and L values used for the V_{th} variability study.

According to Pelgrom's rule, the V_{th} standard deviation, $\sigma(V_{th})$, depends inversely on the square root of the device area, equation (1), where A_{Vth} parameter is related to the device technology. For fixed values of L (L_{cte}) or W (W_{cte}), eq (1) can be written as eq(2) or eq (3), respectively.

$$\sigma(V_{th}) = \frac{A_{Vth}}{\sqrt{W \cdot L}} \quad (1)$$

$$\sigma(V_{th}) \cdot \sqrt{L_{cte}} = \frac{A_{Vth|L}}{\sqrt{W}} \quad (2)$$

$$\sigma(V_{th}) \cdot \sqrt{W_{cte}} = \frac{A_{Vth|W}}{\sqrt{L}} \quad (3)$$

Fig 1 shows the $\sigma(V_{th})$ fitting (lines) of the experimental data (symbols) to eq (2) and eq (3), when only W (left) or L (right) is varied for N- (blue) and P- (red) MOSFETs. Note the different slopes, $\Delta V_{th}|L$ and $\Delta V_{th}|W$, (Table II), which point out a deviation from eq(1) [4], and that different dependences for W and L should be considered. This result is observed for both nMOS and pMOS devices.

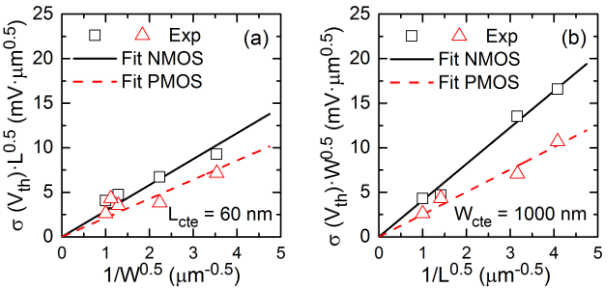

Fig. 1. Experimental σV_{th} (dots) as a function of $1/W^{0.5}$ (a) and $1/L^{0.5}$ (b). The lines correspond to linear fittings, with slopes in Table II.

	$A_{Vth\|L}$	$A_{Vth\|W}$
nMOS	$2.906 \cdot 10^6$ (mV · µm)	$4.088 \cdot 10^6$ (mV · µm)
pMOS	$2.138 \cdot 10^6$ (mV · µm)	$2.517 \cdot 10^6$ (mV · µm)

Table II: Slopes of the linear fittings of the data in Figure 1, to equations (2) and (3).

To elucidate the physical origin of the different observed dependences, TCAD simulations were performed. Since V_{th} variability has been commonly associated to the discreteness of charge [5], in these simulations, discrete fixed charges (DFC) were introduced at the device interface, which are known to modify the device V_{th} [6].

For simplicity, only one DFC was introduced and its impact on V_{th} studied. The DFC was swept along the channel length (Fig. 2a) and channel width (Fig. 2b) of the device, on devices with several geometries. Note that the impact of the DFC on the V_{th} depends on the location of the trap along the channel L (especially for the shorter L's), whereas it is almost independent on its location along W (for all the Ws). This asymmetry in the V_{th} impact, depending on the trap location along W or L, can be the root of the differences observed in Fig 1.

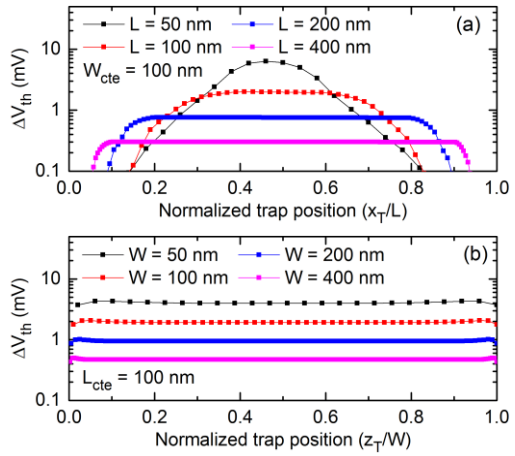

Fig. 2 TCAD simulation of the change in the device V_{th} (ΔV_{th}) when a DFC is swept along the channel length (a) and width (b) of the device. Devices with several dimensions are considered, so that the normalized trap location is plotted in the x-axis.

For a better fitting of the data, the dependences of V_{th} variability on W and L have been decoupled, proposing equation (4) to describe the V_{th} variability. In this expression α and β are free fitting parameters that are used to take into account the different dependences of $\sigma(V_{th})$ on L and W.

$$\sigma(V_{th}) = \frac{B_{Vth}}{W^{\alpha} \cdot L^{\beta}} \qquad (4)$$

Experimental data were fitted (not shown) to (4) and (1), and the α, β, A_{Vth}, B_{Vth} parameters were calculated. In addition, in order to compare the fittings, R-square coefficients were estimated (see Table III). For nMOS and pMOS devices, lower error is obtained when (4) is employed.

	Fit parameters				R-square	
	α	β	A_{Vth}	B_{Vth}	Eq (1)	Eq (4)
unit	-	-	mV·μm	mV·$\mu m^{5/6}$	-	-
nMOS	0.342	0.493	$2.95 \cdot 10^6$	$4.03 \cdot 10^5$	0.907	0.994
pMOS	0.329	0.578	$2.15 \cdot 10^6$	$3.89 \cdot 10^5$	0.816	0.897

Table III: Slopes of the fittings of the experimental data in Fig. 1 to equations (1) and (4).

Note that α and β values can be approximated to 1/3 and 1/2, respectively, for both transistor types. Therefore, equation (5) is proposed to describe the V_{th} dependence of the variability on the geometry of the device, which improves the fitting of our data to the Pelgrom's rule, and avoiding the introduction of new parameters.

$$\sigma(V_{th}) = \frac{B_{Vth}}{\sqrt[3]{W} \cdot \sqrt{L}} = \frac{B_{Vth} \cdot \sqrt[6]{W}}{\sqrt{W \cdot L}} \qquad (5)$$

Fig. 3 (symbols) shows the V_{th} variability as a function of the inverse of the square root of the device area and the fittings (lines) of the experimental data to both models (the one proposed in this work, red line, eq. (5), and Pelgrom's law, blue line). Fig. 3a and 3b show nMOS and pMOS data, respectively. As it can be seen, for both kind of devices, eq. (5) reproduces better the experimental data, obtaining a better fit for nMOS (R-square of 0.99 compared to 0.895 for pMOS). Therefore, taking into account equation (5), the V_{th} variability increase is larger when L dimension is reduced.

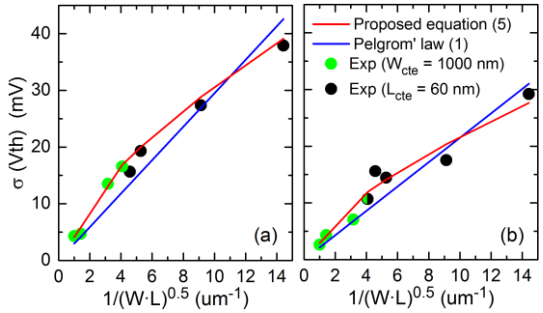

Fig. 3 Comparison between the proposed equation (5) (red line), Pelgroms' law (blue line) and experimental data for nMOS devices (a) and pMOS devices (b). Different colors in experimental data indicate devices with the same; W = 1000 nm (green) or L = 60 nm (black).

III. Conclusions

Our experimental results, as other works, point out a deviation from Pelgrom's scaling rule of V_{th} variability. The W and L dependences have been decoupled and an empirical equation (4) has been proposed, which better describes our experimental observations. TCAD simulations suggest that the different W and L dependences can be related to the V_{th} contribution of traps, which depends on their location in the channel.

Acknowledgment

This work has been partially supported by the Spanish MINECO and ERDF (TEC2013-45638-C3-R) and the Generalitat de Catalunya (2014SGR-384).

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