Mechanical simulations of BOX creep for strained FDSOI

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Abstract

The 'BOX creep' technique consists in introducing stress in a SOI layer by taking advantage of the viscosity of the buried oxide at high temperature. In this study, we deeply investigate the impact of the structure geometry and parameters on the efficiency of creep through mechanical simulations. We find that a 1.1GPa stress can be achieved for an active length of 400nm. This result shows that BOX creep can be an efficient way to boost the performance of future FDSOI technology generations.

Introduction

For the past decade, CMOS performance increase with dimension scaling has been relying on the introduction of boosters [1]. Among them, the use of strained channel is one of the most efficient technique. Especially, compressive and tensile stresses boost hole and electron mobility, respectively. nMOS performance is highly enhanced by using a sSOI substrate [2]. However, it raises a co-integration issue since such a substrate degrades pMOS performance [3]. In order to locally introduce tensile stress, the "BOX creep" technique has been proposed [4]. This technique relies on the creep of the buried oxide at high temperature in order to transfer the strain from a SiN layer (Fig.1). Performance gains have been experimentally demonstrated [5]. Experimental measurements on SOI pFET show a higher current with BOX thanks to the stress introduction (Fig.2). In order to more extensively assess the interest of the BOX creep technique, we deeply investigated its efficiency through mechanical simulations. First, the simulation details are given and the BOX creep mechanism is explained. Then, the structure geometry and parameter impacts are systematically evaluated. Finally, the compatibility of BOX creep with SiGe channel is discussed.

Simulation details

The process flow of the BOX creep technique is as follow: starting from a SOI substrate with 20nm BOX, a pad oxide is deposited before a stressed SiN layer. The active areas are then defined by etching. A high temperature anneal enables the BOX creep thanks to the low viscosity of SiO_2. The SiN layer is finally removed after STI filling and CMP. The simulated half structure, which considers symmetry axes, is given in Fig.3. The values of the simulation parameters including material properties are given in Fig.4. The conditions of reference consist in an anneal of 10min at 1100°C, an active length L_{act}=400nm, and a SiN layer of t_{SiN}=80nm initially stressed at σ_0=-3GPa. The viscosity model used for the simulations consists in a generalized Garofalo's model [6] based on Eyring's one [7], [8] (Fig. 5). The model parameters (η^0 and σ_{crit}) are calibrated on results from literature [9].

BOX creep mechanism

The longitudinal stress σ_{xx} mappings obtained along the different process steps give an insight of the effect of the BOX creep (Fig.6). During the anneal, the low viscosity of the BOX under shear stress enables the relaxation of the stress in the SiN layer and a strain transfer into the SOI layer. This behavior is highlighted on Figs.7 and 8, showing the stress mappings and profiles, respectively, for different anneal durations. After a certain time, the stress in SOI decreases. There is thus an optimized anneal duration, which is found to be dependent on the active length L_{act} (not shown). This behavior will be discussed in the following. After SiN removal, a significant amount of stress remains in the SOI layer (Fig.9). The level of longitudinal stress reaches σ_{xx}=1.1GPa at the center (x=0) in the conditions of reference.

Impact of structure geometry and parameters

By carefully tuning the deposition conditions, initial SiN stress ranging from -3.0GPa to 1.6GPa can be obtained. Fig.10 evidences a good linearity between the initial stress in SiN and the level of stress finally obtained after the BOX creep module at the center (x=0) and under the conditions of reference. As a consequence, BOX creep can be used to induce either tensile or compressive stress. The impact of the SiN layer thickness is reported in Fig.11, showing a saturation for SiN thicknesses above 20nm. This is because a thick enough SiN totally relaxes and thus fully transfers its lattice deformation (i.e. strain) into the SOI.

The role of pad oxide and layout effect

During the anneal, not only the buried oxide but also the pad oxide creep; this due to their reduced viscosity. The pad oxide creep results in a relaxation of the SiN stress without transferring the strain into the SOI. This is the reason why the SOI stress decreases after a certain anneal duration (see Figs.7 and 8). Consequently, the thinner the pad oxide, the higher the stress in the SOI layer (Fig.12). Furthermore, without any pad oxide, a +0.8GPa improvement is achieved for a L_{act}=100nm scaled active region. This is translated into the layout effect (Fig.13). With a 2nm-thick pad oxide, the stress strongly reduces for short active areas while a high stress is maintained without pad oxide.

BOX creep and SiGe integration

For pMOS, a high compressive stress can be obtained by integrating SiGe in the channel, e.g. thanks to SiGe enrichment [10]. In order to introduce an additional compressive stress, a tensely stressed SiN layer must be used. Fig.14 shows that without a pad oxide, it is beneficial for active lengths longer than 200nm (350nm with a pad oxide, respectively).

Conclusion

Thanks to a large set of mechanical simulations, we evidence the best configuration to achieve high stress with the BOX creep technique. Especially, 1.1GPa tensile stress can be generated from a -3GPa compressive nitride, which makes this technique relevant for electron mobility enhancement, in complementary to a SiGe channel for pMOS.

Acknowledgments

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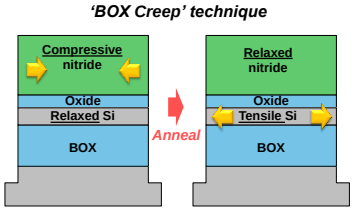

Fig.1. Principle of the BOX Creep technique: transfer of the stress from a SiN layer into the SOI by the means of an anneal at high temperature.

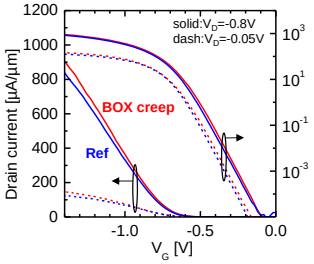

Fig.2. pFET drain current demonstrating the impact of the BOX Creep. Width is W=170nm, gate length is L=20nm and active length is L_{act}=498nm.

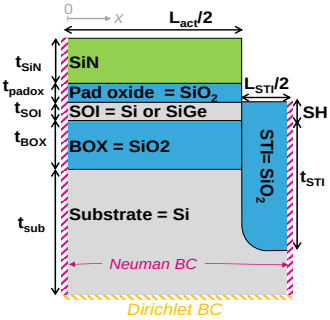

Fig.3. Scheme of the half structure used for the mechanical simulations.

Conditions of reference

Anneal	
Duration	10min
Temperature	1100°C

Materials properties	E <110> (GPa)	ν <110>	CTE (/K)	Stress (GPa)
SiN	280	0.25	3.0 10^{-6}	-3
SiO2	73	0.17	1.37 10^{-6}	/
Si	169	0.063	3.0 10^{-6}	/
SiGe25%	161	0.055	3.0 10^{-6}	-1.6

Parameter	Value (nm)
t_{SiN}	80
t_{padox}	2
t_{SOI}	6
t_{BOX}	20
t_{sub}	174
t_{STI}	100
SH	6
$L_{act}/2$	200
$L_{STI}/2$	20

Fig.4. Tables summarizing the details of the simulation parameters.

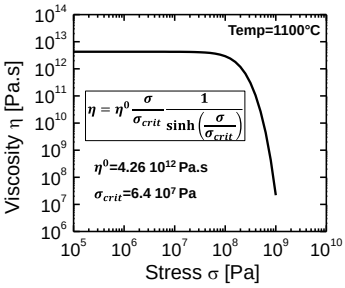

Fig.5. SiO_2 viscosity model at T=1100°C used for the simulations. The model is based on Garofalo's model [6-9].

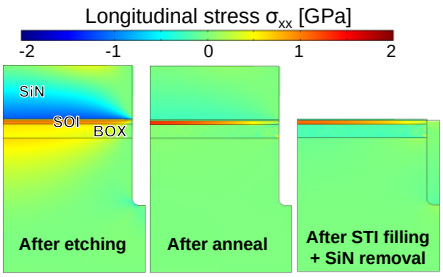

Fig.6. Stress mapping for the different steps of the process. After anneal, the compressive stress in SiN top layer decreases. After removal the SOI layer is tensely stress.

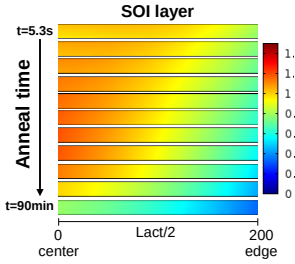

Fig.7. Stress mapping in the SOI film for different anneal durations (from t=5.3sec to t=90min, time is multiplied by 2 from step to step).

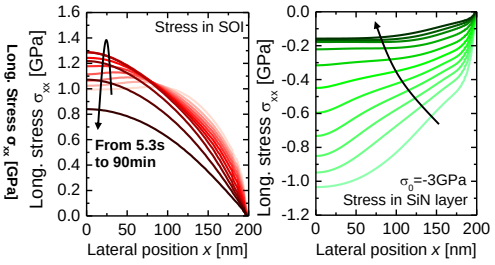

Fig.8. Stress profiles in the *(left)* SOI, in the middle of the film and *(right)* SiN, at 3nm above the bottom of the film. Compressive stress in SiN relaxes and is transferred into tensile stress in SOI.

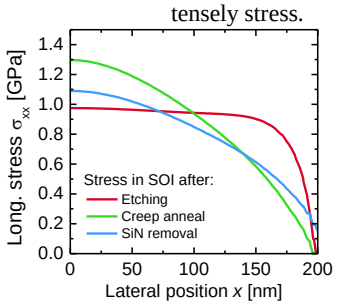

Fig.9. Stress profile in SOI during the process steps. The BOX creep generates a tensile stress in SOI, which is maintained after SiN removal.

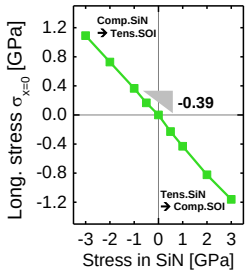

Fig.10. Impact of initial stress in SiN on the level of stress achieved after BOX creep. Good linearity observed.

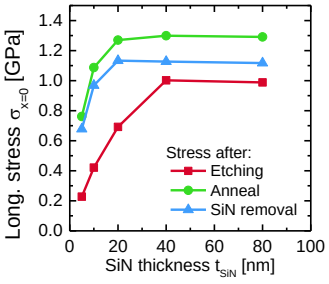

Fig.11. Impact of SiN thickness. Saturation of the final level of stress in the SOI.

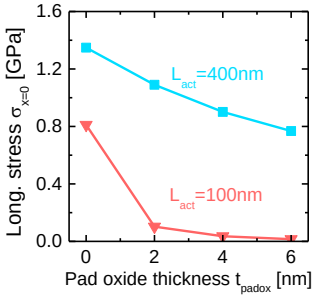

Fig.12. Impact of pad oxide thickness for two different active lengths. Strong impact of the presence of a pad oxide for Lact=100nm.

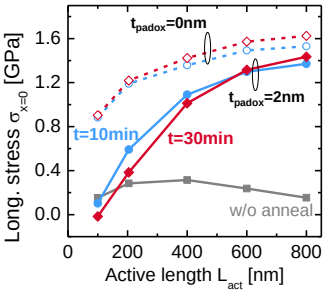

Fig.13. Impact of the layout dimension. Loss of efficiency for short active lengths mainly due to the creep of the pad oxide as stress is highly increased without pad oxide.

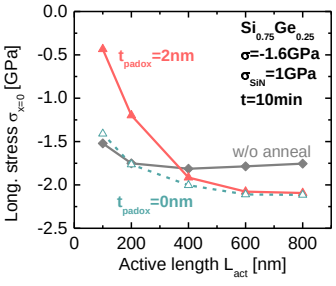

Fig.14. Impact of BOX creep on a SiGe channel and with a *tensile* SiN. Additional comp. stress is observed for L_{act}>350nm with a pad oxide (L_{act}>200nm without the pad oxide).

Impact of cryogenic temperature operation on static and low frequency noise behaviours of FD UTBOX nMOSFETs

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***Abstract*— Unusual peak in the transconductance $g_m(V_{GS})$ characteristics may be observed at 10 K and 77 K operation for an applied gate voltage around 1.1 V. The origin of this behavior was addressed using additional low frequency noise (LFN) measurements. Low frequency noise spectroscopy was performed around 77 K in order to identify active traps located in Si film.**

UTBOX; low frequency noise; cryogenic temperature.

I. INTRODUCTION

Fully depleted (FD) Ultra-Thin Buried Oxide (UTBOX) transistors are considered as promising structures for future CMOS node generations thanks to their enhanced performances. In particular, the thin body offers an improved control of the short channel effects and the non-intentionally doped channel provides better mobility and low variability [1]. The enhancement of device performances expected at very low temperature operation may be accompanied by the appearance of some parasitic effects [2]. Low temperature studies may reveal new information enabling a better understanding of the charge transport and fluctuations. However, up to now, DC and noise in UTBOX devices at very low temperature, i.e. 10K, have rarely been investigated [3].

In this work, an unusual transconductance peak was evidenced at low temperature operation for an applied gate voltage of about 1.1 V. Low frequency noise measurements are also used to give additional input on the origin of this phenomenon. Further, a detailed characterization in terms of short channel effects, analog operation parameters and LFN performances at very low temperature operation will be addressed.

II. DEVICES

The tested devices are FD SOI UTBOX transistors fabricated on 300 mm wafers at imec. They present a fixed gate width W_G (1µm), variable gate lengths L_G (from 120 nm up to 1 µm), a BOX thickness (T_{BOX}) of 10 nm and a silicon film thickness (T_{Si}) of 20 nm. The gate stack consist in a 1 nm interfacial SiO_2 below 2.5 nm high-κ dielectric (SiON), resulting in an equivalent oxide thickness (EOT) of 2.6 nm.

III. RESULTS AND DISCUSSION

Typical transconductance characteristics $g_m(V_G)$ recorded for several gate lengths at 10 K operation are shown in Fig.1. For the shortest gate lengths (i.e. L_G of 120 nm and 170 nm), a transconductance valley can be clearly observed near threshold operation. This behavior may be related to electron filling subbands at very low temperature near threshold and could be observed only if the energy qV_D of the drain voltage and the thermal energy k_BT (about 860µeV at 10K) are not much higher than the energy separation between subbands [4]. As expected, this valley cannot be observed at 77 K (right inset in Fig.1).

An unusual transconductance peak can also be observed in strong inversion (Fig.1). This behavior is also temperature dependent: it becomes attenuated at 77 K to completely disappear at room temperature. As this trend appears in the same applied gate voltage range (i.e. about 1.1 V) whatever the channel length is, in first instance it may be related to the linear kink effect (LKE). However, LKE effect may be unusual in our case because the back gate is grounded. Additional hypothesis may be considered: tunneling effect through dopants diffused from source/drain extensions in the channel [3] or high turn on of the source diode at very low temperature operation [5].

In FD devices, LKE effect may occur when the back gate is in accumulation and it is accompanied by an excess Lorentzian noise mechanism [6]. The exponential dependency of the Lorentzian time constant (τ) versus V_{GT} ($\tau \propto \exp(-\beta \cdot V_{GT})$, β is the exponential coefficient, $V_{GT} = V_G - V_{TH}$, where V_{TH} is the threshold voltage) associated to LKE noise and observed in standard UTBOX transistors from [6] is about 4.5 V^{-1}.

Typical evolution of the frequency normalized noise spectral density is represented in Fig. 2. As observed, the noise behavior can be perfectly modelled by a sum of white noise, 1/f noise and Lorentzian contributions, and the parameters corresponding to each type of noise can be identified (inset equation in Fig. 2).

It can be observed from the inset of Fig. 2 that at 10 K and for $V_G = 1.1$ V (V_{GT} of 0.58 V) no Lorentzian contribution that may be related to LKE noise has been observed. The absence of LKE noise was observed only for extentionless UTBOX devices [6], which is not our case. Moreover, the exponential evolutions of the Lorentzian time constant with V_{GT} observed in strong inversion present an increase of the exponential coefficient from ($\beta \approx 6\ V^{-1}$) at 77 K to ($\beta \approx 8.9\ V^{-1}$) at 10 K operation. However, in the case of the LKE related effect, no (significant) variation of the β with temperature is expected [7]. For traps located in the oxide depth, β is in the range of 25-35 V^{-1} [8]. Furthermore, these Lorentzians (β about 4-6 V^{-1} at 77 K and about 8-9 V^{-1} at 10 K) may be attributed to traps located in the Si film, which may present a bias dependence due to the very thin film thickness [9].

Contrary to LKE and high turn on of the source diode related effects expectations, no clear hysteresis may be observed for the unusual peak between forward and inverse measurements mode (Fig.1).

Traps for which the time constant is independent on the applied voltage are also evidenced (T3 at 10 K from the inset of Fig.2 and T4 at 77 K from Fig. 3). The temperature evolution of the time constant of these Lorentzians allows to identify traps located in the Si film [9]. Even if few points are used, from the Arrhenius diagram (inset of Fig.3), traps related to carbon, boron and oxygen were identified around 77K [10].

Identification of traps related to boron around 77 K using LFN spectroscopy, plus the presence of traps located in the Si film and active in strong inversion at 10 K and 77 K may corroborate with the hypothesis of a tunneling effect through dopants diffused from source/drain extensions in the channel. However, some slope discontinuities on $g_m(V_{GS})$ characteristics were expected to be highlighted also in moderate inversion. Further investigations in 4.2 K -77 K temperature range will permit to clearly identify the origin of this unusual transconductance peak observed in strong inversion.

IV. CONCLUSION

In this work, an unusual transconductance peak was highlighted at cryogenic temperature operation in strong inversion. Different hypothesis on the origin of this phenomenon was discussed through analysing output transfer characteristics and LFN measurements. Most likely, it may be attributed to a tunnelling effect through dopants diffused from the source/drain regions in the channel.

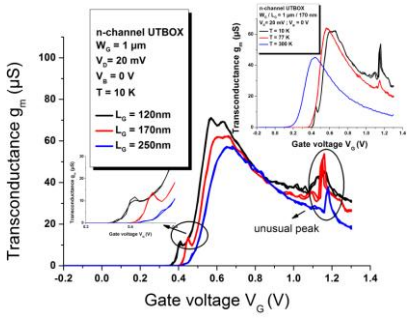

Figure 1. Typical $g_m(V_G)$ in forward and inverse mode at 10 K operation for different channel gate length. The left inset shows $g_m(V_{GS})$ oscillation near threshold. $g_m(V_G)$ behavior at 10 K, 77 K and 300 K is illustrated in the right inset for a channel gate length of 170 nm.

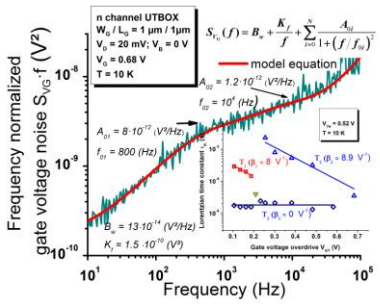

Figure 2. Modelling of a noise spectrum. In the inset: Lorentzian time constant evolution versus V_{GT}.

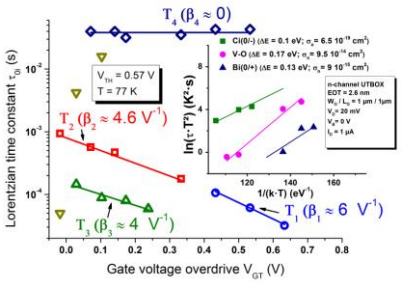

Figure 3. Evolution of the estimated time constant of Lorentzian contributions on the total noise for a transistor operated at 77 K. In the inset: Arrhenius diagram using time constants which are independent of the applied gate voltage.

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