Properties of III-V Nanowires: MOSFETs and TunnelFETs

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***Abstract*—This paper describes the properties and performance status of vertical III-V nanowire transistors. The development of key process modules has advanced the vertical fabrication technology and competitive device performance is reported for InAs MOSFETs and TunnelFETs. Besides the benefits in electrostatic control and the ease in integration on Si substrates, the vertical transistors offers a path towards 3D device integration as demonstrated by the stacked track-and-hold circuit where a capacitor is integrated on top of the vertical transistor for area reduction.**

Keywords—III-V nanowires; III-V MOSFETs; InAs; InAs//GaSb; TFETs

I. INTRODUCTION

The properties of III-V nanowire transistors have shown a dramatic increase in performance that last few years. Part of this improvement is related to the advantageous intrinsic transport properties of III-V materials, but part is also related to the continuous refinement of the processing technologies, what enables the transistor fabrication. The small nanowire volume makes the transistors not only susceptible to surface effects such as scattering, but the structures are also sensitive to contact formation and high-*k* integration in the non-planar geometry. It is hence essential to address these technological challenges and to establish processing techniques supporting the transistor evolution.

In this paper, we will present an approach to optimize various processing technology modules for vertical III-V nanowires including ohmic contact formation, high-*k* integration, and a gate-last technology. The evaluation and optimization is performed in a vertical process flow, what makes the technology directly compatible with the transistor fabrication. These process modules are used to fabricate vertical MOSFETs and TunnelFETs with competitive performance on Si substrates.

II. PROCESSING MODULES

A. Ohmic Contact Formation

Transmission line measurements are a well established approach to characterize ohmic contacts to semiconductors. However, the conventional technique applied to lateral structures is hardly applicable for vertical nanowire structures, since it requires that the contact distance can be changed in a systematic way. Spin-coating and other deposition methods typically results in uniform thickness across the wafers, what limits the usefulness of a single step. Recently, spin-coating of hydrogen silsesquioxane (HSQ) and subsequent electron beam exposure has been developed for vertical nanowire structures as a way to control the spacer layer thickness within the structures [1]. It allows for fabrication of layers with a systematic and well-controlled change of the thickness, and hence the contact spacing, on the same sample, what is required for contact evaluation.

The method has been applied to Ni/W/Au contacts to vertical InAs nanowires with a diameter of about 20 nm. The data show that a low specific contact resistance of 0.6 $\Omega\mu m^2$ and a contact transfer length of about 50 nm can be achieved for these vertical structures [2]. The data is encouraging as it suggests that sufficiently low contact resistance can be achieved also for these comparably thin vertical structures.

B. High-k Integration on Vertical Nanowires

The integration of high-*k* dielectrics on III-V materials is challenging due to the complex nature of the interface oxides and the thermal instability of the sub-oxides. III-V nanowires naturally consists of a multitude of different facets with corners and edges, what may affect the binding of the oxide to the semiconductor. Furthermore, the nanowires are resistive what affects the measured frequency-dependent capacitance and may easily lead to misinterpretation about the material properties.

The RF-properties of InAs/HfO_2 vertical nanowire capacitors were studied for structures with air-bridge finger gates to reduce the parasitic capacitance towards the substrate [3]. Capacitors based on InAs nanowires grown with different growth conditions and with different doping levels were measured to evaluate the influence of the crystal quality and the surface properties on the InAs/HfO_2 interface. The data show a D_{it} minimum around the InAs conduction band edge with minimum levels evaluated to be below 10^{12} $eV^{-1}cm^{-2}$ for samples grown under optimized conditions [4]. Furthermore, doping of the nanowire top segment is found to influence the interface properties on the nanowire side walls, possible due to parasitic growth on the facets. Optimization of the growth conditions was found to be effective in reducing the influence of the doping on the side facets what is critical to reduce the D_{it}.

C. Vertical Gate-Last Technology

Processing of the layers in a vertical geometry typically starts with deposition of the bottom layers followed by the subsequent layers towards the top of the device. However, due to the high resistance in thin nanowires and the challenging ohmic contact formation, a self-aligned, gate-last process was developed [5]. In this flow, a sacrificial HSQ-mask is first applied at the bottom of the nanowire while the nanowire top is covered by the ohmic contact. A recess gate is formed by local etching of the nanowire to trim the diameter after removal of the fist mask. The gate stack is then deposited and the gate-length defined by removal of the gate stack on the top of the nanowire. This process allows for multiple gate lengths on the same sample as it is defined by the edge of the top contact that is controlled by the initial HSQ exposure dose.

III. Applications

A. Vertical III-V MOSFETs

The gate-last processing modules developed have been used to fabricate vertical InAs MOSFETs. Transistors (L_g=190 nm) with I_{on} of 140 µA/µm for I_{off}=100 nA/µm have been demonstrated based on a subthreshold swing of 90 mV/dec. The highest transconductance reported for these transistors were g_m=1.6 mS/µm. Substantial increase in performance is expected as these transistor still are limited by the top contact access resistance, what may be minimized by the optimized ohmic contact scheme described above. These vertical transistors may find applications for CMOS at scaled nodes, where the vertical direction is used to provide more space for gates and separation layers as compared to lateral transistors, what saves power [6]. Evaluation has also shown that these transistors may show competitive performance at millimeter wave frequencies, once the parasitics are controlled [7].

B. 3D Device Integration

The vertical nanowire geometry naturally allows for vertical device stacking where individual transistors and other components are connected in the vertical direction. This approach saves space on the substrate although it requires demanding processing as well as layout considerations to identify the best options for the device integration. As a first step towards a 3D device integration scheme, a capacitor was integrated on top of a vertical InAs nanowire MOSFET forming the basis for a track-and-hold circuit [8]. This circuit was selected since it requires quite a large capacitor to match the input in the subsequent circuit blocks. The capacitor was wrapped around the transistor top contact and the functionality of the track-and-hold circuit demonstrated. Evaluations showed that 10*x* capacitor area saving can be achieved for 400 nm long nanowires when places at 100 nm spacing.

C. III-V TunnelFETs

The possibility to grow nanowire heterostructures offers a wide range of possibilities to design structures suitable for TunnelFET fabrication. For nanowire TunnelFETs, the electrostatic control is essential and hence the diameter needs to be scaled to about 20 nm or below [9]. InAs/GaSb nanowire TunnelFETs have shown very high current levels as the broken band alignment provides little resistance at the heterojunction. However, no subthreshold swing below 60 mV/decade was detected [9]. Adjusting the material composition at the heterojunction to InAs/GaAsSb/GaSb improves the device transfer characteristics to below 60 mV/decade operation [10]. Still, comparably high I_{on}=10 nA/µm was measured at V_{ds}=0.3V. The data suggest that indeed TunnelFETs with competitive performance can be realized and there is no reason to believe that the performance can not be increased further by improved heterostructure design and enhanced electrostatics.

IV. Summary

This work describes the recent advancement in processing technology for vertical III-V nanowire MOSFETs and TunnelFETs, including ohmic contact formation, gate-stack formation, and gate-last processing. These modules are essential for the realization of transistors with competitive performance both for digital and millimeter wave applications.

Acknowledgment

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Vertically Stacked Lateral $Si_{80}Ge_{20}$ Nanowires Transistors for 5 nm CMOS Applications

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***Abstract*— In this work we present a simulation study of $Si_{80}Ge_{20}$ vertically stacked lateral nanowires transistors (NWTs) with potential application at 5nm CMOS technology node. Our simulation approach is based numerous simulations techniques in order to capture the complexity of such ultra-scaled device. We have used ensemble Monte Carlo (MC) simulations in order to accurately predict the drive current taking into account the complexity of the carrier transport in the NWTs. We have used also drift-diffusion (DD) simulations with quantum corrections based on Poisson-Schrodinger solution in order to accurately calibrate the density-gradient based DD quantum corrections. Finally we have benchmarked the current in $Si_{80}Ge_{20}$ NWTs against Si based NWTs.**

Keywords- Nanowire Transistor, TCAD, Monte Carlo.

I. INTRODUCTION

Excellent electrostatic integrity offered by gate all around nanowire transistor renders them one of the more prominent candidates for reaching the ultimate CMOS scaling limits. Different from FinFETs, the nanowire transistors have stronger quantum mechanical effects due to the small diameter and the surrounding oxide barrier, which has to be taken into account accurately in simulations [1]. The non-equilibrium transport phenomena including quasi-ballistic effects require predictive Monte Carlo simulations. In addition the trade-off between performance and leakage currents can be achieved by engineering the device structures. The electron transport properties in (NWTs) could be precisely engineered to reach the industrial target of improving the saturation current by 15% (for each generation) by introducing strain in the channel, and by using various device cross-section geometries and channel orientation. Adopting Si_xGe_{1-x} alloys as a channel material, can lead to further improvement of the performance of nanowire transistors (NWT). Fig 1 compares the 3D schematic view of the 14nm FenFET and Single, Double, Triple 5nm nanowire transistors (NTWs).

II. METHODOLOGY

In this work Monte Carlo (MC) transport simulations with Poisson-Schrödinger (PS) quantum corrections are used as a reference point for a single NWT. We have calibrated our drift-diffusion (DD) simulations to this reference results. A simplified workflow is presented in Fig.2. The (DD) simulations have been employed for studying the performance of multiple channel NWTs in the presence of contact resistance and for studying the statistical variability (SV).

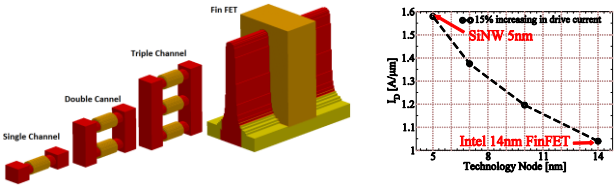

Fig. 1 (right) 3D schematic view of the Fine of Intel 14nm FenFET and Single, Double, Triple 5nm Si nanowire transistors (NTWs) and (left)the scaling target from 14nm technology to 5nm technology.

In the (Poisson-Schrödinger (PS) / Drift-Diffusion (DD)) simulations suitable mobility models are used to represent the vertical and lateral field dependence of the mobility and to allow calibration to the MC results. Previous simulations have shown that for <110> orientation nanowires with elliptical cross section have better electrostatics performance compared to circular, rectangular and circular cross sections. The NWT structure in this work has three elliptical 5nmx7nm lateral nanowires as shown in fig 3. Fig 4 shows the wavefunctions in the fold and four-fold degenerate valley in the 2D cross-section of 5nmx7nm lateral Si NWT (V_G=0.70V).

III. RESULTS AND DISCUSSIONS

Based on the methodology described in the previous section we have compared in Fig. 5 I_D-V_G characteristics, 14 nm FinFET [4] with a single Si-NWT simulated in this work. Also those results are compared to the target drive current (1.58 mA/µm) for the 5 nm CMOS. From the results presented in Fig. 5 is clear that saturation current for single Si nanowire transistor is higher in comparison to 14nm FinFET. This conclusion is valid for both high and low drain biases. More importantly, Fig. 5 reveals that even though that the single NWT has better drive current the value of the I_{sat} is significantly lower in comparison to our target value of 1.58 mA/µm at 5nm CMOS technology node both for low (5mV) and high (0.7V) drain biases.

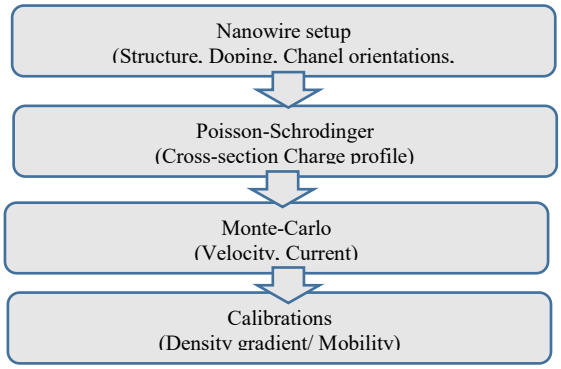

Fig2: The simulation tool calibration flow chart

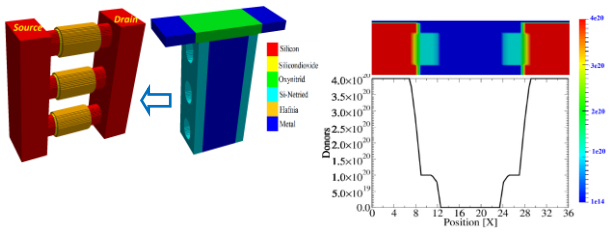

Fig 3- 3D schematic view a vertical stacked lateral (NWTs) and material information. (left) The doping profile of the single lateral NWT.

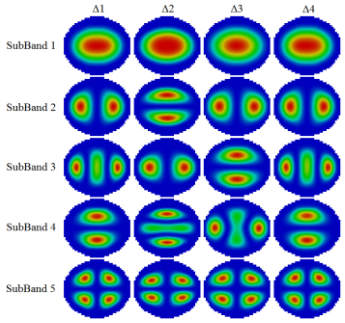

Fig. 4 Wavefunctions in the fold and four-fold degenerate valley in the 2D cross-section of a circular Si NWT (V_G=0.70V).

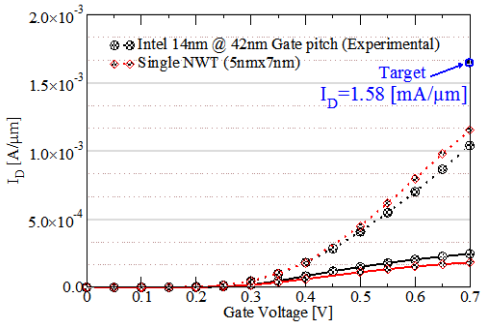

Fig. 5 I_D-V_G curve compares the experimental performance of Intel 14nm FinFET with the 5nm silicon Nanowire (MC simulations). Dashed lines correspond to high drain voltage V_D=0.7V, while the solid lines are for low drain voltage V_D=0.05V. The gate length of NWT is 12 nm.

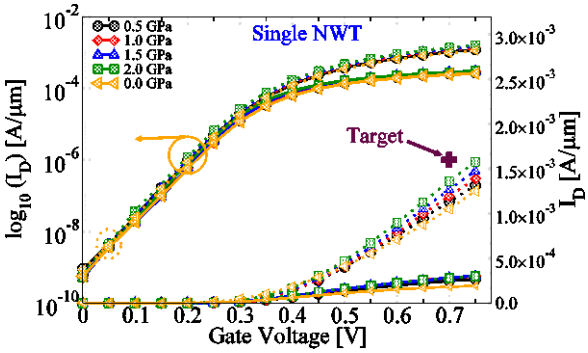

Fig. 6 I_D-V_G curve compares results for 5nm silicon Nanowire transistor with a single channel at four different channel stains (MC simulations). Dashed lines correspond to high drain voltage V_D=0.7V, while the solid lines are for low drain voltage V_D=0.05V. The gate length is 12

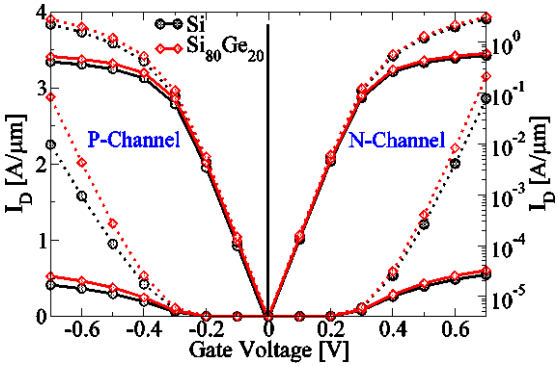

Fig. 7 I_D-V_G curve compares results for 5nm x7nm Si80Ge20 vertically stack three lateral NWT transistor PMOS and N-MOS (without strain). Dashed lines correspond to high drain voltage V_D=0.7V, while the solid lines are for low drain voltage V_D=0.05V. The gate length is 12nm

A possible option to improve the I_{sat} current is to introduce stain in the channel. Simulation of the Id-Vg characteristics of a single NWT with four different strain values is presented in Fig. 6. It is clear that introducing channel strain indeed improves the I_{sat} value but still the target drive current cannot be reached even at 2.0 GPa stain. Another option to improve I_{sat} is to introduce vertically stacked lateral NWTs as one device [3]. Introducing multiple channels is technologically challenging but possible. Although, the vertical stacking of three lateral Si NWT is a satisfactory to exceeds the industrial targets in term of saturation current for N-MOS, P-MOS suffers from low hole mobility. One possibility is to replace the Si channel with $Si_{80}Ge_{20}$. Fig. 7 shows I_D-V_G characteristics for 5nmx7nm Si channel and $Si_{80}Ge_{20}$ channel for PMOS and NMOS NWT with three lateral channels. Clearly the inclusion of SiGe can help to achieve the performance target at 5nm CMOS.

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Static and LF noise characterization of ultra-thin body InAs MOSFETs

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***Abstract*—A complete static and low frequency noise characterization of ultra-thin body InAs MOSFETs is presented. Characterization techniques established for Si MOSFETs are applied in order to extract the electrical parameters and study the behavior of these research grade devices.**

Keywords-Electrical characterization, III-V materials, InAs MOSFETs, Low-Frequency Noise, Random Telegraph Noise

I. INTRODUCTION

The necessity of pursuing Moore's Law while surpassing the limitations of Silicon, led to the study of new materials and processes for metal oxide semiconductor transistors. For example, III-V materials like InAs and InGaAs are widely regarded as leading candidates for increased drive current digital applications. The accurate determination of the electrical parameters in such novel devices is essential for understanding their physical properties. In this context, the goal of the paper is to apply characterization techniques that are already established for Si MOSFETs in order to study the behavior of ultra thin body InAs MOSFETs.

II. EXPERIMENTAL DETAILS

The devices measured in this work are ultra thin body (UTB) InAs MOSFET transistors with MBE selectively raised InAs n+ Source/Drain (S/D) contacts on lattice mismatched InP/InAs/InGaAs/InAlAs/InP epi-layer [1]. The high k gate stack is composed of Al_2O_3 (2 nm) and HfO_2 (2 nm). The capacitance equivalent thickness of the structure (CET) is around 1.7 nm. The channel length L varies from 1 μm down to 0.025 μm while the channel width W is fixed at 3 μm. Drain current measurements in the linear region (V_D = 30mV) were performed with Agilent B1500 Semiconductor Device Analyzer, whereas the drain current noise was measured using the Agilent B1530 Waveform Generator Unit.

III. RESULTS AND DISCUSSION

A. Parameter Extraction

Typical I_d-V_g characteristics at V_d = 30 mV are presented in Fig. 1 both in linear and logarithmic scale for different gate lengths. In order to extract the device parameters, we applied the Y-Function method (Eq. 1) in strong inversion for several gate lengths (see Fig. 2) [2].

In a previous work, it has been shown that the Lambert-W (LW) function can describe very well the inversion charge Q_i (Eqs. 2-4) from weak to strong inversion [3]. V_d is the drain voltage, μ_{eff} the effective mobility, and θ_1, θ_2 the mobility attenuation factors. Indeed, we applied the methodology described in [3] to verify the applicability of this method in these experimental level devices. Impressively, as shown in Fig. 1, using the best fit parameters we managed to have a very good agreement between the experimental and the modeled $I_d(V_g)$ curves from weak to strong inversion. As can be seen in Fig. 3, the threshold voltage V_t and low-field mobility μ_0 values extracted from LW lie close enough to those obtained from Y-function, yet being reasonably unequal, concerning the fundamental differences of the two methods. The ideality factor obtained from the LW function methodology is in very good agreement with the one directly deduced from the maximum sub-threshold slope (see Fig. 4). The fast interface trap density can be deduced from the ideality factor as $N_{it} = C_{ox}/q.(n-1)$, providing values in the range $3\text{-}6.10^{13}$ /eVcm^2. Additionally, from the θ_1-G_m slope we found the series resistance equal to $R_{SD} \approx 310\ \Omega\cdot\mu m$, which is a reasonably good value for such UTB III-V devices.

B. Low–frequency Noise characterization

Fig. 5 shows the measured normalized drain current power spectral density at f = 2 Hz, where the spectrum is 1/f-like, for all the different channel lengths. This noise trend typically indicates carrier trapping/de-trapping in gate oxide defects near the oxide/semiconductor interface, leading to carrier number fluctuations (CNF) and correlated mobility fluctuations (CMF) [4]. Indeed, as shown in Fig. 6, the CNF/CMF model (Eqs. 5-7) can well describe the LFN for the devices under study. S_{Vfb} is the flat-band voltage power spectral density, λ the dielectric tunneling constant (≈ 0.1nm), kT the thermal voltage, f the frequency, N_{st} the slow oxide trap areal density, α_{sc} the Coulomb scattering coefficient, μ_{eff} the effective mobility, C_{ox} the oxide capacitance per unit area and Ω the CMF coefficient. By fitting the noise results with the CNF/CMF model, we extracted the oxide trap density $N_{st} \approx 2\cdot10^{13}$ /cm^2/eV, in line with the fast trap density obtained from subthreshold slope. The Coulomb scattering coefficient was found to be $\alpha_{sc} \approx 4\cdot10^3$ V·s/C, a typical value for good quality semiconductors. Moreover,

in small length devices such as L = 0.05 µm, high-amplitude Random Telegraph Noise was also observed (see Fig. 7), originating from individual traps within the gate oxide.

IV. Conclusion

A complete static and LF noise characterization of UTB InAs MOSFETs has been performed. The electrical parameters of these research grade devices were investigated, demonstrating high mobility for the long channel devices. The lower values of μ_0 corresponding to short channel transistors and the high interface trap density reveal that further process optimization of these transistors is required.

Acknowledgment

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$$Y = I_d / \sqrt{g_m} \quad (1) \qquad I_d = \frac{W}{L}\mu_{eff} Q_i V_D \quad (2) \qquad Q_i(V_g) = C_{ox} \cdot \frac{nkT}{q} \cdot LW\left(e^{\frac{q\cdot(V_g - V_t)}{nkT}}\right) \quad (3) \qquad \mu_{eff} = \frac{\mu_0}{1 + \theta_1 \frac{Q_i}{C_{ox}} + \theta_2 \left(\frac{Q_i}{C_{ox}}\right)^2} \quad (4)$$

$$\frac{S_{Id}}{I_d^2} = \frac{g_m}{I_d^2} S_{Vfb}\left(1 + \Omega \frac{I_d}{g_m}\right)^2 \quad (5) \qquad S_{Vfb} = \frac{q^2 kTN_{st}}{WLC_{ox}^2 f^\gamma} \quad (6) \qquad \Omega = \alpha_{sc}\mu_{eff} C_{ox} \quad (7)$$

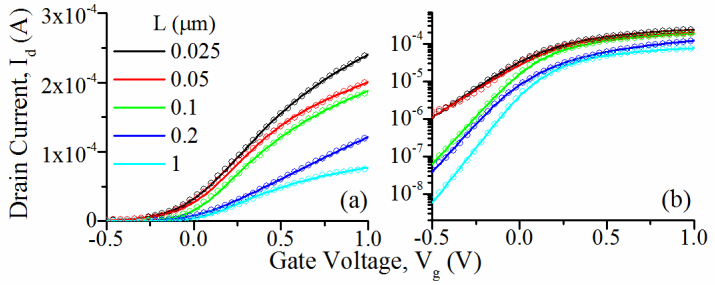

Figure 1. Experimental (symbols) and LW-fitted (lines) transfer characteristics for UTB InAs n-MOSFETS.

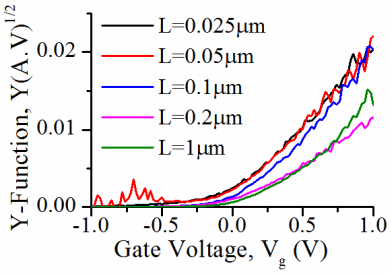

Figure 2. Y-V_g characteristics for UTB InAs n-MOSFETS.

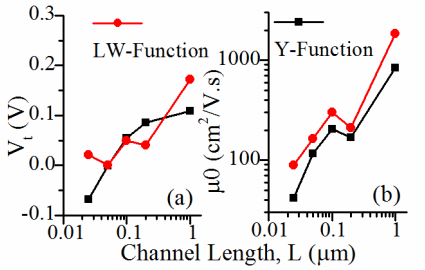

Figure 3. Variation of V_t (a) and μ_0 (b) extracted from Y-Function (black lines) and LW-Function (red lines) with L.

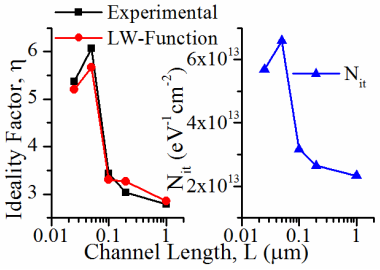

Figure 4. Variation of η extracted experimentally (black lines) and from LW-Function (red lines) and N_{it} with L.

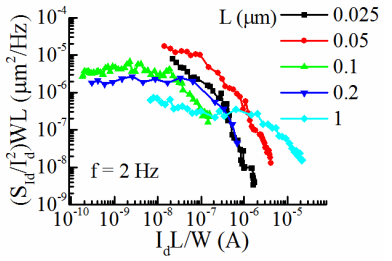

Figure 5. Normalized drain current noise as a function of the normalised drain current for different channel lengths.

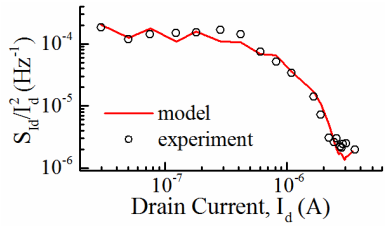

Figure 6. Normalized drain current noise (symbols) and CNF/CMF model fitting (line) versus drain current for L = 0.1 µm.

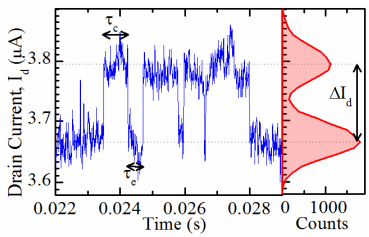

Figure 7. Example of RTN measurement for L = 0.05 µm and V_g = 40 mV.

Analysis of the transistor efficiency of Gas Phase Zn Diffusion $In_{0.53}Ga_{0.47}As$ nTFETs at different temperatures

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Abstract

In this work, the influence of the temperature and the different equivalent oxide thickness (EOT) of $In_{0.53}Ga_{0.47}As$ nTFETs fabricated with gas phase Zn diffusion is analyzed. The different devices have in their gates stacks 3 nm of HfO_2 (with an EOT of 1 nm) or 2 nm of HfO_2 (with an EOT of 0.8 nm). The use of an EOT of 0.8 nm increases the band-to-band tunneling generation and also improves the subthreshold region characteristics, presenting a sub 60 mV/dec minimum subthreshold swing (56 mV/dec) at room temperature, resulting in better efficiency in weak conduction. Considering the temperature influence, the on-state current is less affected than the off-state current due to the band-to-band tunneling mechanism. In the subthreshold region the temperature decrease, which strongly reduces the off-state current, allows the band-to-band tunneling current to be more dominant, resulting in a better subthreshold swing and, consequently, a better transistor efficiency in the weak conduction regime. The opposite behavior occurs when heating the devices, reducing the influence of the band-to-band tunneling in the subthreshold region, degrading both the subthreshold swing and transistor efficiency in the weak conduction regime. In the strong conduction regime, the transistor follows the transconductance tendency, increasing for higher temperatures.

Introduction

Tunnel Field Effect transistors (TFET) are gated p-i-n diodes, where the main carrier injection mechanism is Band-to-Band Tunneling (BTBT) [1]. For low power/low voltage applications, TFETs are promising alternatives due to the subthreshold swing (SS) that can be lower than the theoretical limit of the conventional MOSFET (60 mV/dec) [2-4], as already demonstrated in [5].

One disadvantage of the Si TFETs is the low on-state current (I_{ON}) caused by the large and indirect bandgap (E_G). The use of different materials with lower E_G, as Si_XGe_{1-X} alloys [6-9] and III-V materials [10,11] to enhance I_{ON} is widely studied .

Although TFETs were designed to boost the switching characteristics for low power, they also show good potential for analog applications [12-19].

Temperature analysis of TFETs , is helpful in order to understand the impact of the different conduction mechanisms on parameters, like, in the case of this work, the transistor efficiency (gm/I_{DS}), which is an important analog parameter. In this work, the influence of the temperature and the different equivalent oxide thickness (EOT) of $In_{0.53}Ga_{0.47}As$ nTFETs fabricated with gas phase Zn diffusion is analyzed experimentally on the subthreshold swing, the activation energy of I_{ON} and the transistor efficiency .

Device Characteristics

The devices used in this work are n-type $In_{0.53}Ga_{0.47}As$ homo-junction TFETs fabricated in imec, Belgium, using Zn gas phase diffusion in the source. These devices are based on the original approach from the University of Tokyo [11,20] using spin-on-glass (SOG) diffusion, further optimized by Alian et al. in [21] using solid-source diffusion, and in [22] using gas phase diffusion. The schematic representation of the used $In_{0.53}Ga_{0.47}As$ devices is shown in figure 1.

Two different splits were analyzed, with a gate stack composed of 3 nm or 2 nm of HfO_2 on top of 1nm of Al_2O_3, with TiN as the metal gate. The devices with 3 nm of HfO_2 present an equivalent oxide thickness (EOT) of 1 nm and the devices with 2 nm present an EOT of 0.8 nm. The P++ source is doped with Zn using gas phase diffusion and the drain is doped with Si (N++). More details about the process can be found in [22].

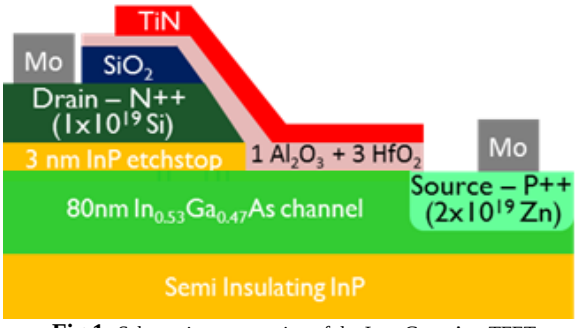

Fig.1–Schematic cross section of the $In_{0.53}Ga_{0.47}As$ nTFET.

Experimental Results and Discussion

The experimental normalized drain current (I_{DS}/W) as a function of the gate voltage (V_{GS}) for both studied EOTs at different temperatures is presented in figure 2. From this figure, it is possible to observe that the temperature, for both devices, affects more the off-state current (I_{OFF}) than I_{ON}.

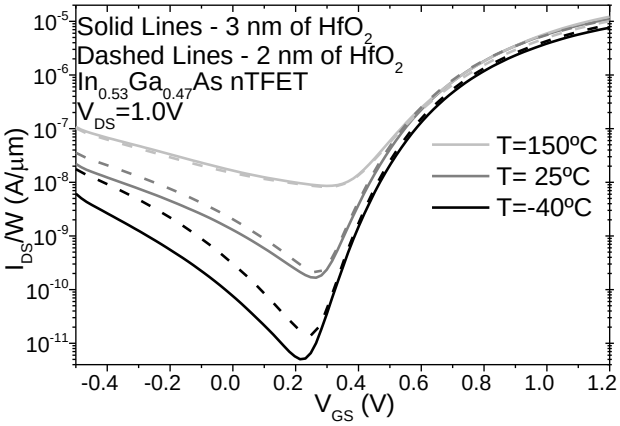

Fig.2–Experimental I_{DS} vs V_{GS} at different temperatures of $In_{0.53}Ga_{0.47}As$ nTFETs with EOT of 0.8 nm and 1.0 nm, respectively.

This behavior can be explained by the current components of I_{OFF}. I_{OFF} is mainly composed by trap-assisted-tunneling (TAT) and Shockley-Read-Hall generation (SRH), which, according to Eqs (1) and (2) exhibit a thermally activated temperature dependence, much stronger than for BTBT [23], which is the dominant conduction mechanism of I_{ON}. Because of this I_{OFF} presents a higher dependence on temperature than I_{ON},. According to Eq. (3), the lower temperature dependence of the BTBT mechanism is mainly caused by the bandgap reduction with the temperature [24-26]. In contrast to MOSFETs, both I_{OFF} and I_{ON} of TFETs increase with higher T.

$$J_{SRH} \cong C1_{SRH}.e^{\left(-\frac{\frac{E_g}{2}+(E_d-E_i)}{k.T}\right)} \quad (1)$$

$$J_{TAT} \cong C1_{TAT}.e^{\left(-\frac{\frac{E_g}{2}+(E_d-E_i)}{k.T}\right)} \quad (2)$$

$$J_{BTBT} \cong \frac{C1_{BTBT}}{E_g}.e^{\left(-C2_{BTBT}.\frac{E_g^{3/2}}{\xi}\right)} \quad (3)$$

where J is the current density, $C1_{SRH}$, $C1_{TAT}$ and $C1_{BTBT}$ are pre-exponential constants for the simplification of the expressions, E_g is the bandgap, E_d is the defect energy level, E_i is the intrinsic energy level, k is the Boltzmann constant, ξ is the total electric field and $C2_{BTBT}$ is an exponential constant for the J_{BTBT} simplification.

Analyzing the effect of the EOT reduction, one can observe an increase of the control of the current, notably in the subthreshold region, due to the increase of the electrostatic control of the gate over the channel. This behavior can also be observed in the activation energy (E_a), presented in figure 3. In this figure it is possible to note that, besides that all devices suffer from a high series resistance, which tends to reduce E_a, the activation energy is lower for the low EOT device, which indicates that it is more in the BTBT regime, due to the better coupling.

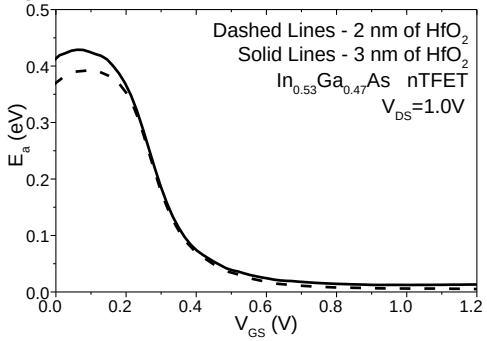

Fig.3–Experimental E_a vs V_{GS} at different temperatures of $In_{0.53}Ga_{0.47}As$ nTFETs with EOT of 0.8 nm and 1.0 nm, respectively.

The better electrostatic coupling can be also observed in the subthreshold swing (SS) curve (figure 4). It is noticeable that the minimum SS (SSmin) in the 2 nm HfO_2 device is lower for all temperatures, which is caused by a better electrostatic coupling. One observes that at room temperature the SSmin of the 2 nm of HfO_2 device is 56 mV/dec, while the 3 .nm device reaches 60 mV/dec. For lower temperatures, as I_{OFF} is reduced, the BTBT is dominant for lower V_{GS} values, where SS is lower, resulting in a reduction of the SSmin. On the other hand, when increasing the temperature, I_{OFF} is increased, suppressing BTBT for low V_{GS} and degrading SSmin.

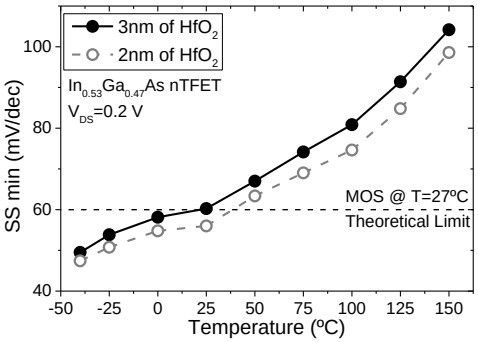

Fig.4–Experimental SSmin vs temperature of $In_{0.53}Ga_{0.47}As$ nTFETs with EOT of 0.8 nm and 1.0 nm, respectively.

One of the most important analog parameters is the transistor efficiency (gm/I_{DS}). The gm/I_{DS} curve can be analyzed in two different regions, one in strong conduction and the other in weak conduction. In the weak conduction region, the efficiency is inversely related to the SS. At lower temperatures the SSmin is improved, consequently increasing the transistor efficiency, however the SSmin degradation at high temperatures causes a decrease of the efficiency. In the strong conduction region, the transconductance is the dominant factor. In this region, which can be better seen in the inset of figure 5, the opposite behavior can be observed. At lower temperature the transconductance is reduced, causing a degradation of the efficiency. At higher temperatures the transconductance is increased, due to the improvement of the tunneling mechanism, boosting the transistor efficiency.

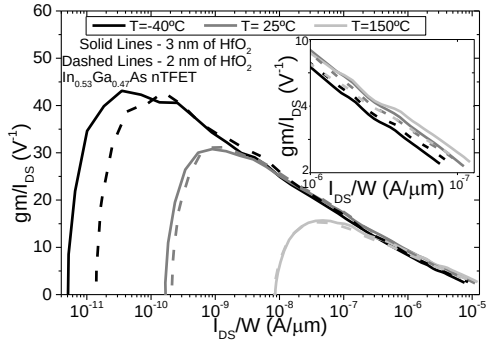

Fig.5–Experimental gm/I_{DS} vs I_{DS}/W at different temperatures of $In_{0.53}Ga_{0.47}As$ nTFETs with EOT of 0.8 nm and 1.0 nm, respectively.

Conclusions

In this work, the analysis of the analog transistor efficiency of $In_{0.53}Ga_{0.47}As$ nTFETs fabricated with gas phase Zn diffusion at different temperatures is performed for the first time. Two different splits were analyzed, one with 1.0 nm of EOT and the other with 0.8 nm. The device with 0.8 nm of EOT presented better electrostatic coupling, which improves the subthreshold region and the BTBT generation.

The temperature has a higher influence on I_{OFF} than on I_{ON} due to the low temperature influence on the BTBT conduction mechanism (I_{ON}). The main temperature influence on the subthreshold region is the I_{OFF} suppression or increase, which allows the BTBT to be more or less dominant in the subthreshold region. This behavior reduces (improves) the SSmin for lower temperatures and increases (degrades) SSmin for higher temperatures. This behavior is also reflected in the transistor efficiency for the weak conduction regime, which is inversely related to the SS. In the strong conduction regime the transistor follows the transconductance tendency, increasing for higher temperatures.

Acknowledgment

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