The Prospects of Two-Dimensional Materials for Ultimately Scaled CMOS

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***Abstract*—Over decades, MOSFET gate length scaling has been the main source of progress in semiconductor electronics. Today, however, the motivation of the industry to continue gate length scaling is declining. On the other hand, researchers still spend considerable efforts on reducing the gate length and on developing ultimately scaled MOSFETs. To this end, both new device architectures and alternative channel materials are investigated. In the present paper, the future of CMOS scaling in the light of emerging 2D channel materials is discussed.**

Keywords—MOSFET scaling; 2D materials ; end of scaling

I. Introduction

Over decades, MOSFET gate length scaling has been the major driver in semiconductor electronics. In commercial circuits, the gate length has been reduced from about 5 µm in 1975 down to sub-50 nm in 2005 as shown in Fig. 1. This translates into an exponential gate length reduction, accompanied by an exponential growth of the number of transistors integrated on a single Si chip, a trend colloquially called Moore's Law.

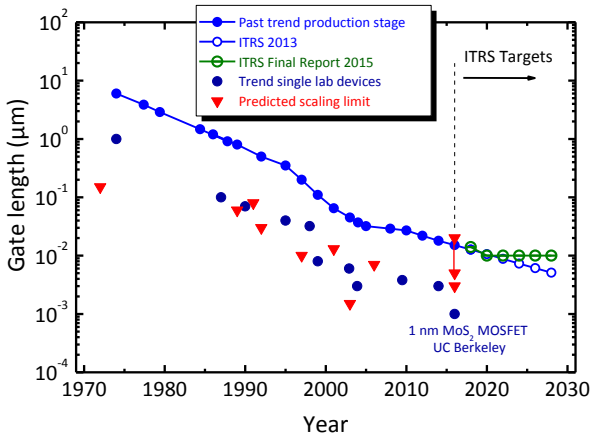

Fig. 1. Evolution of gate length scaling. After [1], updated.

Scaling was substantially supported by a regularly updated roadmap called ITRS (International Technology Roadmap for Semiconductors) [2]. The ITRS served as valuable guideline to keep semiconductor electronics on the path of Moore's Law by continuous gate length scaling.

During the past few years, however, the situation has changed [3-4] and contradictory trends can be observed. On the one hand, the interest of the industry to proceed with gate length scaling is fading away and the importance of the ITRS is declining. On the other hand, in the lab device engineers have achieved remarkable progress in gate length scaling and well-performing ultra-scaled MOSFETs with sub-5 nm gate lengths [5] have been reported. The most recent bang was the demonstration of a 1-nm gate MOSFET with 2D (two-dimensional) MoS_2 channel [6].

II. A Skeptical Perspective on Scaling

By implementing multiple-gate MOSFET architectures into baseline CMOS, leading chipmakers found a way to follow Moore's Law without necessarily scaling the gate length. Furthermore, over the years the expenses for leading-edge chip fabs skyrocketed and today only four companies (Intel, Samsung, TSMC, and GlobalFoundries) fabricate chips at the most advanced technology nodes compared to about 20 companies 15 years ago [7]. Since each of these companies has its own roadmap, the idea of an international roadmap with over 1000 people involved in its preparation has become obsolete. In 2013, the last regular ITRS edition has been published and the more than 20-year success story of the ITRS finally came to an end with the publication of the rather rudimentary final ITRS report in 2015 [2].

The diminishing interest of the industry in continuing gate length scaling has also to do with dramatic changes in the semiconductor market. High-performance logic chips, e.g., fast processors, do no longer represent the most important market segment. Instead, circuits for mobile applications, where low power consumption is more important than performance and where gate length scaling is not necessarily beneficial, have become major drivers.

III. An Optimistic Perspective on Scaling

For decades, Si has been dominating the semiconductor world. However, the pioneering work on the preparation of graphene in 2004 [8-9] brought a new class of solids, the two-dimensional materials (2DMs), into the focus of research. Despite exceptional electronic properties like its ultra-high mobility μ, graphene could not live up to the high expectations due to its zero band gap E_G. Meanwhile, however, hundreds of 2DMs beyond graphene are under investigation, see Fig. 2.

Some of the 2DMs combine the ultimate thinness of graphene with a sizable E_G and therefore are potentially useful for transistors. Yet, thin semiconducting channels are not the only compulsory condition for proper operation of ultimately scaled CMOS. Likewise, a sufficiently heavy carrier effective mass m_{eff} is needed to suppress direct source-drain tunneling at ultra-short gate length levels.

The 2DMs currently under investigation offer a wide range of E_G and m_{eff}. Although there is no wonder 2DM meeting all requirements of ultimately scaled CMOS, several 2DMs are very promising for 5 nm and below gate length levels.

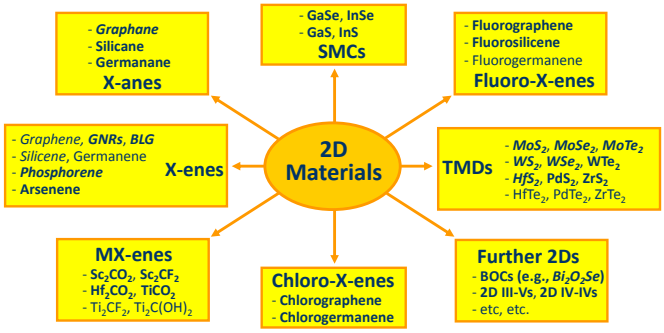

Fig. 2. Classes and representative examples of 2DMs. SMC: Semimetal chalcogenide. GNR: Graphene nanoribbon. BLG: Bilayer graphene. TMD: Transition metal dichalcogenide. BOC: Bismuth oxychalcogenide. Materials in bold letters: 2DMs with bandgap. Materials in italic letters: 2DMs already used in experimental FETs. After [10], updated.

In 2016, a 1-nm-gate n-channel MOSFET with 2D MoS_2 channel has been reported [6]. This device showed excellent switch-off, an on-off ratio around 10^6, a minimum subthreshold swing *SS* of 65 mV/dec, an average *SS* of 115 mV/dec over 5 decades of drain current variation, and no indication of serious source-drain tunneling, thus proving that 1 nm does *NOT* represent the physical limit for gate length scaling. The electron m_{eff} in MoS_2 is around $0.46\times m_0$ (m_0 is the electron rest mass) compared to $0.26\times m_0$ for Si, $0.12\times m_0$ for Ge, and $0.06\times m_0$ for GaAs [11-12]. We note that the introduction of heavy-m_{eff} materials into CMOS would mark a radical paradigm shift since so far the industry favors light-m_{eff}, high-μ channel materials to improve the on-state behavior of transistors for digital CMOS [1].

We have used the quantum-mechanical simulator NanoTCAD ViDES [13-14] to investigate source-drain tunneling in ultra-scaled MOSFETs. To this end, we simulated double-gate MoS_2 MOSFETs and intentionally varied the electron effective mass while keeping all other parameters constant. As can be seen in Fig. 3, for $m_{eff} \geq 0.2\times m_0$ excellent subthreshold behavior (*SS* < 70 mV/dec) and a good suppression of source-drain tunneling and short channel effects are obtained for a gate length of 5 nm.

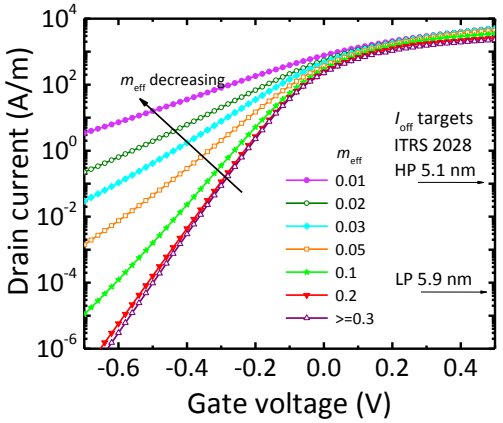

Fig. 3. Simulated transfer characteristics of 5-nm double-gate MOSFETs with channels showing different m_{eff}.

In accordance to the experimental results from [6], our simulation of a 1-nm gate MoS_2 MOSFET shows that even for such short gate length levels excellent switch-off and sufficiently good subthreshold characteristics with *SS* below 100 mV/dec and reasonable drain-induced barrier lowering can be achieved.

IV. Conclusion

In the recent past, the warning voices that gate length scaling would slow-down and come to an end soon went louder and gained acceptance. As we have shown, however, the physics-governed limits of gate length scaling are still far. There are, however, many other issues. First of all, reliable processes for the fabrication of transistors on a large scale with ultra-short gate length, e.g., a production-stage sub-5 nm lithography, must be available. Second, variability issues will be crucial in these transistors. Regarding the 2DMs, the formation of good ohmic contacts and a dedicated doping scheme need to be installed. Moreover, the unsatisfying long term stability of the 2DMs needs to be conquered.

We conclude that research on 2DMs is still in its infancy and that it is impossible to make a serious prediction if 2DMs will be able to replace Si. We can state with certainty, however, that the Si MOSFET is approaching its scaling limits, that gate length scaling is slowing down, and that certain 2DMs including MoS_2, phosphorene, and others show promise for ultimately scaled CMOS. On the other hand, we do not expect to see 1-nm gate MOSFETs in production in the near to medium term.

Acknowledgment This work has been supported by a TU Ilmenau Research Grant and a Carl Zeiss Promotion Fund.

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Charge Transport, Interface and Border Traps in Al_2O_3/InGaAs structures

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***Abstract*— The paper focuses on electrical properties and determination of transport mechanism through dielectric layer, surface states in the dielectric/semiconductor interface and border traps in the Pd/Al_2O_3/$In_{0.53}Ga_{0.47}As$/InP MOS system in dependence on gate dielectric thickness. The current appeared to be governed by Fowler-Nordheim tunneling. The potential barrier for electrons at the metal-dielectric interface and the conduction band offset at the dielectric-semiconductor interface have been shown to equal to 2.40±0.10 eV and 2.50±0.06 eV, correspondingly. The optimal value for Al_2O_3 oxide thickness among the MOS structures under study is shown to be 10 nm.**

Keywords: h-k dielectrics; InGaAs; charge transport; border traps; surface states

I. INTRODUCTION

High mobility channel material such as high In-content InGaAs is considered as a potential candidate for replacing strained Si in future high-performance low-power complementary metal oxide semiconductor (CMOS) devices [1]. The use of high-κ dielectric materials in conjunction with III-V substrate is highly required for the demands of future progress and improvement of MOSFET performance in high speed logic and RF applications. In this work we present results of complex electrical characterization of the Me/Al_2O_3/$In_{0.53}Ga_{0.47}As$/InP MOS system focusing on transport mechanism through the dielectric layer, interface and border traps in/near Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface in dependence on thickness of ALD Al_2O_3 thin dielectric layer.

II. EXPERIMENTAL

The devices under study were Me/Al_2O_3/$In_{0.53}Ga_{0.47}As$/InP MOS capacitor structures. High-κ Al_2O_3 oxide layer was formed by atomic layer deposition (ALD) of nominal physical thickness t_{ox} of 5, 10, 15 and 20 nm. Prior to gate oxide deposition the $In_{0.53}Ga_{0.47}As$ surface was passivated by an immersion in 10% $(NH_4)_2S$ solution at room temperature for 20 min. The top Pd or Au/Pt/Ti gate metallization was obtained by a shadow mask process. Samples with both *n*(S)- and *p*(Zn)- type doped ($4x10^{17}cm^{-3}$) $In_{0.53}Ga_{0.47}As$ epitaxial layers were characterized by capacitance-voltage (*C-V*) measurements in frequency range from 10Hz to 2MHz and current-voltage (*I-V*) measurements over the temperature range of 100 – 300 K using an Agilent E4980A Precision LCR meter and Agilent 4156C Precision Semiconductor Parameter Analyzer.

III. RESULTS AND DISCUSSION

A. Charge transport in Me/Al_2O_3/InGaAs srucures

Analysis of I-V characteristics of the structures measured in positive and negative gate voltages shows that the current can be described by Fowler-Nordheim (FN) tunneling [2]. FN plots for forward and reverse branches of the structures with *n*-type substrate are shown in Fig. 1. One can see, that the samples with t_{ox}= 5 nm do not show a well formed barrier for FN tunneling at the interfaces possibly due to the dominating of direct tunneling transport mechanism. For the case of electron tunneling from the metal electrode (Fig. 1a), the barrier height, $\varphi_{B,}$ is the same for the 10, 15 and 20 nm thick dielectric and equals to 2.40±0.10 eV. For the electron tunneling from the semiconductor (Fig. 1b), 10 nm thick dielectric gives the barrier height φ_B =2.50±0.06 eV, that represents the conduction-band energy offset at the Al_2O_3/InGaAs interface [3].

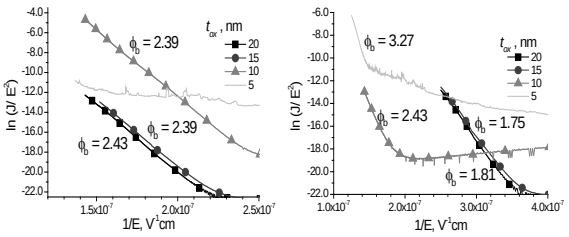

Figure 1. The FN plot for the the reverse bias branch (V_g<0) (a) and forward bias branch (V_g>0) (b) of *J-V* characteristic of Pd/Al_2O_3/*n*-$In_{0.53}Ga_{0.47}As$/InP structure

From Fig. 1b it is evident that the thicker dielectric layers (15 and 20 nm) demonstrate unexpectedly lower values of φ_B and lower electric fields at which tunneling starts. Observed effect can be explained by the existence of deep traps in the dielectric layer at the tunneling distance from the semiconductor-dielectric interface The presence of such traps changes the transport mechanism

from FN tunneling to trap-assisted tunneling (TAT) [4]. In this case the effective barrier height is lowered by the trap depth value. The depths of traps in the transition layer are presented in Table I. It should be noted that the thicker dielectric the deeper traps.

TABLE I. ENERGY LOCALIZATION OF TRAPS IN TRANSITION LAYER OF AL_2O_3

Oxide Thickness (nm)	**E_C-E_{TRAP} n-type substrate (eV)**	**E_C-E_{TRAP} p-type substrate (eV)**
15	0.51	0.60
20	0.59	0.94

B. Surface traps in Al_2O_3/InGaAs interface

In paper [5] it was shown that integral density of surface traps, D_{it}, at room temperature in the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface in the energetic range of $In_{0.53}Ga_{0.47}As$ band gap from E_C-0.04 eV to E_V+0.04 eV can be calculated from shift of V_{FB} for n-type and p-type $In_{0.53}Ga_{0.47}As$ correspondingly using follow expression

$$qD_{it} = C_{OX}(\Delta V_{FBN} - \Delta V_{FBP}), \quad (1)$$

where C_{OX} is the oxide capacitance determined either experimentally from C_{MAX} or from calculation of a geometric capacitance from thickness and dielectric constant (k=8.9 for Al_2O_3 was determined from our experiments). The results, which use both approaches, are presented in Fig. 2. In both cases of the calculations we observe the minimum of surface trap density for oxide thickness about 10 nm.

C. Border traps

The effective border trap density, ΔN_{BT}, can be obtained by integrating the absolute value of the difference between the C-V curves measured in forward and reverse directions [6], that is

$$\Delta N_{BT} = (1/qA)\int \left|(C_{reverse} - C_{for\,var\,d})\right| dV. \quad (2)$$

Using of expression (2) and results of the CV characteristic hysteresis presented in Fig. 3 the effective electron border trap densities for different thickness of the gate oxide were calculated. The CV characteristics hysteresis was measured at the same accumulation electric field. It was shown that effective border trap density has maximum values for the gate oxides with thickness of 15 and 20 nm (see inset Fig.3).

Thus, the $Al_2O_3/In_{0.53}Ga_{0.47}As$ structure with dielectric thickness about 10 nm has a minimal density of surface traps, low concentration of electron border traps and low leakage current with good formed potential barrier between Al_2O_3 and $In_{0.53}Ga_{0.47}As$. Increase of the alumina thickness associated with an increase of time of sequentially layer deposition by ALD technique at enough high temperature that can result to additional diffusion of indium and gallium from semiconductor into dielectric layer. This diffusion leads to surface and border trap formation that can increase tunnel current injection into the gate dielectric.

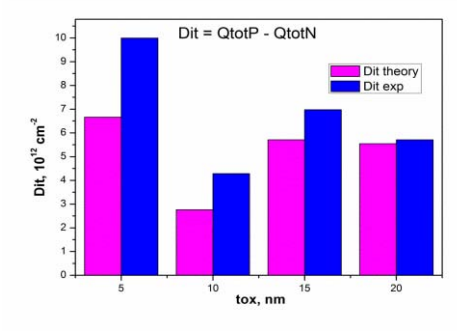

Figure 2. Integral density of surface traps in the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface vs. thickness of Al_2O_3.

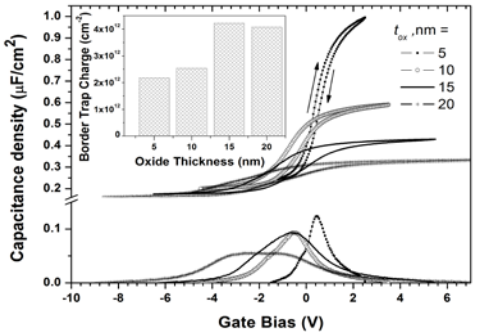

Figure 3. C-V characteristics of the $Pd/Al_2O_3/n$-$In_{0.53}Ga_{0.47}As$ structures measured in forward and reverse directions and $C_{forward} - C_{reverse}$ vs. gate voltage for different thickness of the gate dielectric. Inset: Border trap density as a function of Al_2O_3 thickness

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Evaluation of ONO compatibility with high-k metal gate stacks for future embedded flash products

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***Abstract* — Embedded flash memories having high-k metal gate-based logic devices will require modifications of the flash cells in order to remain economically feasible. For 1T NOR cell, one potential integration scheme is keep the traditional ONO layer as the flash cell's integrate dielectric and replace its poly-Si control gate with the same high-k metal gate stack used for the logic devices. Preliminary electrical tests show that an HfSiON/TiN/a-Si gate stack does not significantly impact the EOT or leakage properties of the ONO layer. This stack is more robust than the traditional ONO with a poly-Si gate.**

Keywords; embedded flash, ONO, high-k metal gate, non-volatile memory

I. Introduction

Embedded flash memories (eFlash) involve the co-integration of advanced CMOS (LV) devices with flash memory matrices and the high voltage (HV) transistors necessary for the generation of the pulses required for flash operations. These memories are used in microcontrollers, automotive and smartcard applications under a variety of mission profiles. Due to the technological complexity of their integration, these memories are generally one node behind the latest logic or standalone memory nodes.

Therefore, flash memories embedded with CMOS based on SiO_2 gate oxides and poly-Si gates are evolving towards those based on high-k materials and metal gates (HKMG). In an eFlash processes where the logic and flash devices have their control gates formed simultaneously (typically for the 1T NOR cell), the flash cell may then require modifications in order to accept the HKMG stack in contact with the $SiO_2/Si_3N_4/SiO_2$ (ONO) integrate dielectric.

II. Background

The use of high-k dielectrics to replace the ONO in flash memories to attain lower equivalent oxide thicknesses (EOT) has been of interest since the late 1990s [1]. In the majority of this research, the driving force was the shrinking of the cell size for high-density standalone applications [2]. The move to planar NAND configurations required considerable decreases in EOT to maintain performances and high-k multilayers such as $HfAlO/Al_2O_3/HfAlO$ were developed [3].

In embedded flash memories, the HV circuitry takes up a considerable amount of space on the die; the reduction of the size of these circuits via lower program/erase voltages may be as important as the density of the flash matrix itself. Additionally, the control gate remains wrapped around the floating gate; the sides continue to contribute to the capacitive coupling, reducing the need for very aggressive EOTs.

III. Embedded Flash and Test Wafer Integration

A. Embedded Flash Process Flow

The eFlash fabrication flow is preferentially modular to reduce the interaction between the HV and Flash devices on one side and the LV MOS on the other. The first poly-Si layer simultaneously forms the gates of the HV transistors and the floating gates of the flash. The second poly-Si stack forms the control gates of the flash and the LV logic devices, with the ONO being exposed to the gate oxides of the LV devices [4]. If the LV devices use high-k metal gates, then the flash devices will also comprise a high-k metal gate.

B. Damascene capacitor process flow

Capacitor test structures can be used to screen gate stacks for basic information before attempting the integration with a flash product. Fig. 1 shows a schematic overview of the process flow used to make the 100 µm by 100 µm MOSCAPs. After ion implantation (N+ type) of an n-type Si substrate 550 nm of SiO_2 is deposited. A standard lithography mask is used to define the test structures before the exposed SiO_2 is etched down to the Si. The ONO and gate stack to be tested is then deposited on the wafer, followed by a thick W plug. Chemical mechanical polishing, stopping in the thick SiO_2 layer defines the devices without the need to develop etching procedures.

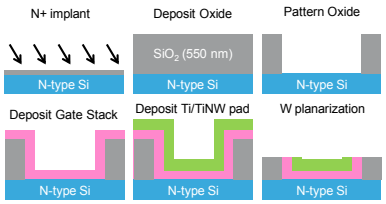

Figure 1: Schematic process flow for damascene capacitors

C. *Devices and testing*

The four capacitor samples are summarized in Table 1. Devices were fabricated on 300mm wafers at the CEA-LETI and STMicroelectronics.

TABLE I. SAMPLE CHARACTERISTICS

	Name			
	Si	***HKMG***	***MG***	***HK***
Dielectric	ONO	ONO	ONO	ONO
1.8nm HfSiON	-	Yes	-	Yes
TiN	-	Yes	Yes	-
Si	Yes	Yes	Yes	Yes
EOT (nm)	11.9	11.5	11.2	12.0

Capacitance, current and time dependent device breakdown (TDDB) measurements were completed on 20 devices. Contact is made by a point to the W-plug and by the chuck to the backside of the wafer.

IV. RESULTS AND DISCUSSION

The CV curves for all samples are shown in Fig. 3. The change from a poly-Si gate to a HfSiON/TiN/a-Si stack leads to a slight decrease in EOT, likely related to the change in permittivity of the IGD as nitrogen from the TiN diffuses into the dielectric. The slight shoulder that appears when TiN is used in the gate is considered to be related to traps introduced by nitrogen from the TiN [5].

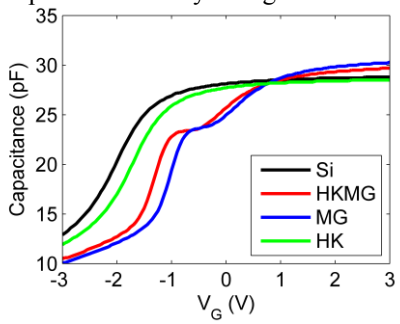

Figure 2: CV curves at 100 kHz for all samples at 25°C, they are not strongly frequency dependent

The IV curves of the ONO samples, shown in Fig. 4, exhibit similar medium and high voltage currents; this implies that the currents are limited by bulk conduction in the ONO. The slightly lower currents at 4-6 V when a metal gate is used are likely related to the slightly reduced oxide field in these cases as the flatband voltage is more positive with the metal gate. It is important to note that direct IV measurements are not sensitive enough to measure leakage currents at the electric fields that are relevant for data retention tests.

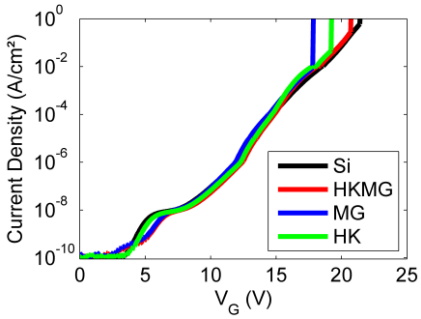

Figure 3: Current density vs voltage at 25°C

The TDDB results for V_G = +17 and 18.5 V are shown in Fig. 5. The switch from a poly-Si gate to a HfSiON/TiN/Si gate increases the time to breakdown.

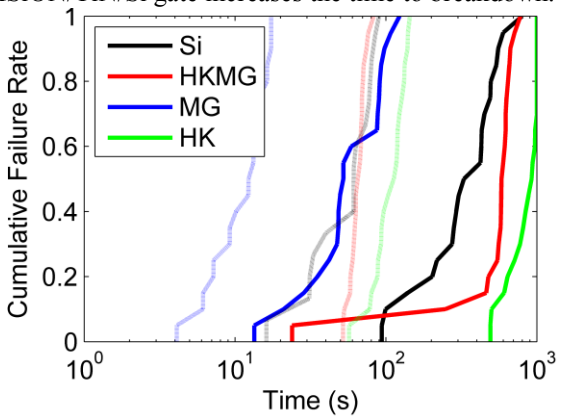

Figure 4: Cumulative failure rate at 125 °C under gate stress of +17 V (solid lines) and +18.5 V (broken lines)

V. CONCLUSIONS

A preliminary analysis of the electrical properties of ONO layers with high-k/metal gate stacks has been completed within the framework of flash memories co-integrated with high-k/metal gate-based CMOS logic for future embedded applications. ONO layers with high-k/metal gate stacks do not show degraded leakage properties and are more robust in time dependent breakdown measurements at 125°C than those made with poly-Si gates.

ACKNOWLEDGMENT

This work was completed with support from the ANRT (Association Nationale de la Recherche et de la Technologie) in the form of a CIFRE Fellowship

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Hydrogen Silsesquioxane Tri-Dimensional Advanced Patterning Concepts for High Density of Integration in sub-7 nm Nodes

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***Abstract*—Recent developments in CMOS devices such as FinFET, FDSOI or stacked nanowire FETs (SNWFETs) have led the industry to consider increasingly complex integration processes while aiming at smaller and smaller devices. This paper proposes new concepts of device integration based on the use of hydrogen silsesquioxane (HSQ). Recently employed to replace polysilicon sacrificial gate in gate last processes, its use could also be extended for building the whole transistor level including device lateral insulation, multi-workfonction layouts, self-aligned contacts and possibly the first layer of metal interconnects. If several EUV masks could be employed for such a use, HSQ patterning once enhanced by multi-electron beam lithography, could allow to perform all these features within a single exposure step without involving any conventional etching or stripping steps.**

Keywords - 3D lithography; HSQ; stacked nanowire FETs; SNWFET; FinFET.

I. INTRODUCTION

In recent years, the use of double gate devices such as FDSOI and FinFET has become necessary to increase the performance while shrinking device and gate length. Stacked nanowire FET (SNWFET) can be considered as an evolution of FinFET gate last integration technology [1-3]. In this work however, an alternative approach to standard gate last practices is proposed. The following integration scheme takes advantage of the unique characteristics of hydrogen silsesquioxane (HSQ). Namely, this non-organic and front-end compatible resist crosslinks into SiO_x oxide after EUV or electron beam (e-beam) exposure. HSQ was first exploited to realize self-aligned sacrificial gate all-around (GAA) SNWFETs since silicon does not hinder HSQ exposure under the NWs [3-5]. This allows to address SNWFETs specific integration issue: the placement of internal spacers in between the vertically stacked NW channels which are essential for reducing parasitic capacitances [1]. Although HSQ sacrificial gates were originally intended to be employed with stacked NWs, the concepts introduced in this abstract are entirely transferable to FinFET integration.

II. NW-FIRST INTEGRATION OF SNWFETS

Stacked NWs are realized from Si/SiGe fins that are patterned into an epitaxial superlattice (Fig 1a&b). In a gate last and NW first integration approach, sacrificial SiGe is removed before sacrificial gate patterning (Fig 1c). The suspended NWs are then immersed into a first HSQ resist layer whose thickness t_1 depends on spincoating speed and solvent viscosity. E-beam through-silicon exposure is then performed in order to define the sacrificial gates (Fig 1d). No conventional etching or stripping is needed since the exposed and developed material becomes the oxide used as a sacrificial gate. Several gates are placed on the same silicon rods: this is particularly beneficial in a NW first approach where Si/SiGe anchors have to be designed on both ends which results in wafer area loss (Fig 1b). For FinFET or NW last approach – in which the sacrificial SiGe is etched away within the gate cavity after the sacrificial gate is removed [1,3] –, this technique also avoids the use of a specific mask to cut off the Si or SiGe for isolating the devices from one another. A second layer of HSQ with a thickness $t_2 < t_1$ is then spincoated. As exposed HSQ is entirely selective to the TMAH developer, device lateral insulation can now be achieved in a similar way (Fig 1e). Gate lateral spacers can then be patterned, source and drain (S/D) fabricated (possibly as described in [1,4]) before device encapsulation in polysilicon (Fig 1f). Similarly as for the poly-open-polish chemical mechanical planarization (CMP) of oxide pre-metal dielectric (PMD) encapsulation, polysilicon CMP stops onto the highest HSQ oxide sacrificial gates. These are then etched away and replaced with the high-k metal gate (HKMG) stack (Fig 1g). SiN stoppers may be implemented involving another CMP. The polysilicon is finally removed (Fig 1h) and S/D contact cavities are filled with tungsten. The last metal CMP is pushed down to the second population of HSQ oxide features that have remained buried until this point. Consequently, transistors are isolated from one another by oxide walls (Fig 1i). Likewise, this approach could provide enough flexibility to address many other issues (Fig 1j&k).

III. CONCLUSION

A new concept of 3D lithography for advanced nodes integration has been introduced from which many implementation variants can be derived. They are based on several HSQ intrinsic properties that allows to conceptualize a new step forward in the device density of integration. Preliminary investigations bring the device pitch within a 30 to 40 nm range. HSQ intrinsic properties could permit to either take full advantage of the upcoming EUV lithography or benefit from the flexibility and nanometric precision of multi electron beam lithography for which the use of HSQ offers to skip many process steps in order to reach a competitive wafer total processing time as compared with usual steppers.

ACKNOWLEDGMENT

This work was partly funded by the French Public Authorities through the NANO 2017 program and by the IBM – STMicroelectronics - CEA/LETI - MINATEC Development Alliance. The authors thank the LETI facilities and Nano-characterization Platform (PFNC) for device processing and characterization and SOITEC for providing SOI substrates.

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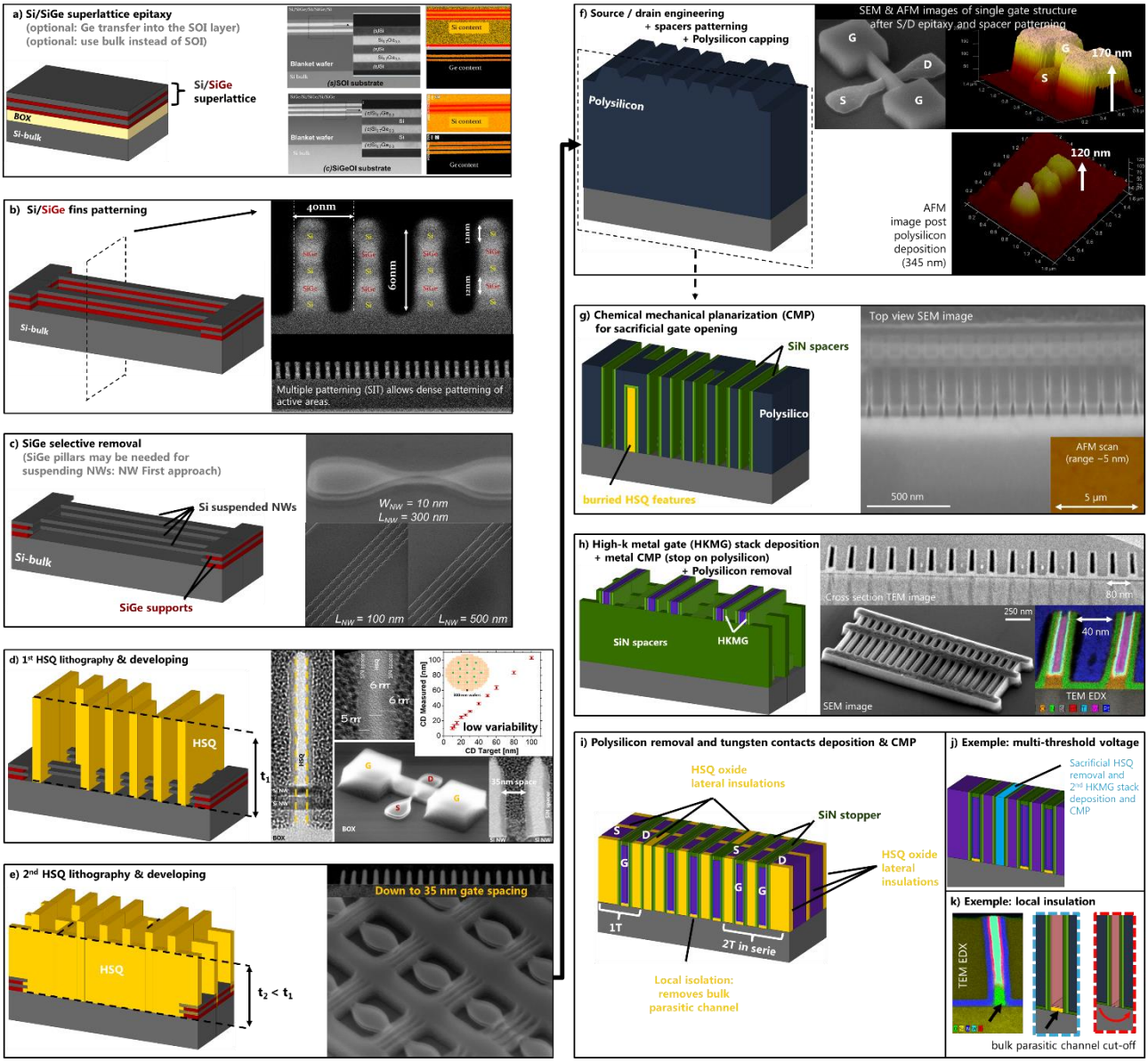

Figure 1. Gate last and NW first integration of SNWFETs: introduction to HSQ 3D lithography.

Si nanowire MOS capacitor characterization model system

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***Abstract*— A model system of Si nanowire (SiNW) Metal Oxide Semiconductor (MOS) capacitors, composed of arrays of vertical Si nanowires of height 1.35 and 2.5 μm respectively, a pitch of 1.4 μm and diameter 0.43 μm, has been fabricated and studied. The gate dielectric was a thermally grown SiO_2 layer, 6 nm thick, and the gate metal was Al. The SiNWs were formed by using photolithography and reactive ion etching. We studied the increase in capacitance density due to the 3-dimensional (3-D) nanostructuring by the SiNW formation and found that it scales quite well with the geometrical increase in capacitor surface area. The exact knowledge of the number of SiNWs on the surface, as well as their homogeneity in size, allowed the extraction of the single SiNW capacitance and intrinsic series resistance. Also, properties such as the density of interface states, the flat band voltage and the voltage at which the nanowire becomes fully depleted are determined.**

Keywords: Si nanowire; MOS capacitor; Si nanowire MOS characteristics; Si nanowire MOS model system

I. INTRODUCTION

3D nanostructuring of Si, including the formation of vertical Si nanowires (SiNWs) or nanopillars on the Si surface, is interesting for many applications in on-chip electronic devices. In the case of metal-insulator-semiconductor (MIS) capacitors, it can be used to increase the effective surface area of the capacitor, and thus increase accordingly the capacitance density. This is very useful in applications in dynamic random-access memory (DRAM) devices, energy storage devices etc. In the above applications, an increase in capacitance density reduces the necessary footprint of the capacitor on the chip, thus reducing the system cost. In SiNW MIS capacitors it is essential to understand the relation between structural and electrical characteristics, in order to be able to design new devices with controlled properties. However, there are only few reports in the literature dealing with the capacitance of a single Si nanowire MIS structure, due to the fact that this capacitance is generally very small and thus difficult to be measure [1-3]. An array of Si nanowires is necessary, in order to get a measurable signal [4, 5]. In such a system, the extraction of single nanowire characteristics can be hindered from a large dispersion in nanowire sizes and the lack of precise control over the number of nanowires present in the capacitor.

In this work we present a model system of SiNWs with reduced size dispersion, used to fabricate model SiNW MIS capacitors. The nanowires were fabricated using advanced optical lithography and Si etching techniques, which allowed their precise location and size control. A thin SiO_2 layer was used as dielectric. The SiNWs were used to create a 3D structure and increase the effective area of the MIS capacitor compared to the same device on a flat Si surface. They were large enough and sparse enough so as to be able to precisely measure their number in the fabricated capacitors. The characterization of this model system allows the extraction of a single SiNW capacitor characteristics in a simple and accurate manner.

II. EXPERIMENTAL

SiNW arrays were fabricated by combining a photolithography step, followed by Si reactive ion etching for pattern transfer to the silicon substrate. To ensure a large scale and cost efficient process, an I-line stepper (FPA CANON 3000i4) has been used to reach a critical resolution of 350 nm at wafer scale.

Two different samples were investigated in this work. They both comprised arrays of vertical cylindrical SiNWs in tetragonal arrangement on the Si surface with a pitch of 1.4 μm, and SiNW diameter of 0.43μm. The height of the nanowires in the first case was 1.35μm, while it was 2.5μm in the second case. A characteristic scanning electron microscopy (SEM) image of the 2.5μm tall SiNWs at 45^o angle is depicted in fig. 1(a). MIS capacitors were fabricated on both flat Si surfaces (planar capacitors) and Si surfaces containing arrays of SiNWs (SiNW capacitors). The gate dielectric was a 6nm thick SiO_2 layer, while the gate metal was a 1μm thick Al layer. Both flat and SiNW MIS capacitors were fabricated on the same wafer with the same process run in order to eliminate process deviations and to provide a more accurate comparison between them.

III. MEASUREMENTS

The fabricated MOS capacitors were characterized

TABLE I. SUMMARY OF THE RESULTS OF THE ELECTRICAL CHARACTERIZATION FOR ALL THREE CAPACITORS MEASURED AT 10^6HZ.

Device type	Device property							
	$C_{total,\ calculated}$ (nF)	$C_{total,\ measured}$ (nF)	C. density ($\mu F/cm^2$)	$C_{depletionn}$ (nF)	R_S (Ω)	V_{FB} (V)	Q	D_{it} ($V^{-1}cm^{-2}$)
Flat	0.89	0.9	0.58	0.017 @-0.7V	38	-0.1	4.6	2×10^{10}
SiNW (1.35μm)	1.70	1.7	1.2	0.018 @-0.8V	41	-0.2	2.3	5×10^{10}
SiNW (2.5μm)	2.10	1.8	1.4	0.018 @-0.8V	44	-0.2	2	2×10^{10}

using well established characterization protocols. An example of capacitance density as a function of applied voltage for all three fabricated devices at a frequency of 1 MHz is depicted in figure 1(b). The main results are summarized in table I. The calculated total capacitance uses a parallel plate model in the case of the flat capacitor, while the case of the SiNW capacitors the total capacitance is the sum of the flat area capacitance and the cylindrical SiNW capacitance by the number of SiNWs. In each SiNW capacitor, the knowledge of the exact number of SiNWs, as well as their size and uniformity, are critical for an accurate result.

IV. RESULTS AND DISCUSSION

From the results presented in table I it can be seen that the measured capacitance is exactly the same as the calculated one in the case of the shorter SiNWs, while there exists a small deviation in the case of the longer ones (almost 15%). This, combined with the precise knowledge of the number of SiNWs on the capacitor surface, allows the experimental determination of a single nanowire capacitance, which is 130pF for the shorter and 240pF for the longer SiNWs.

Using the same reasoning, it is easy to show that the increase in series resistance due to the presence of the SiNWs is due to the intrinsic resistance of the SiNWs themselves. This is measured to be $4.7\text{x}10^{-5}\Omega$ and $1.1\text{x}10^{-4}\Omega$ per SiNW respectively for the two SiNW lengths. This observation is useful in determining the lower limit of series resistance or, equivalently, the upper limit of the cutoff frequency in such SiNW-based devices.

Finally, we should note that the change in flat-band voltage between flat and SiNW capacitors is quite small,

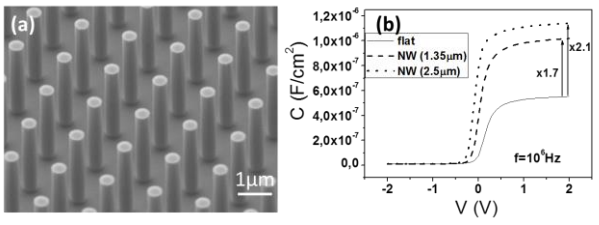

Figure 1. (a) SEM image at 45° angle of the sample with Si NWs of 2.5μm length and a 1.4μm pitch. (b) Capacitance density (C) as a function of applied voltage (V) for all three devices measured at a frequency of 10^6Hz.

which implies that the presence of the SiNWs does not introduce any significant increase in defect states within the dielectric or near the Si/SiO_2 interface. In addition, the measured low density of interface states in all cases suggests that the SiNW surface is quite smooth and does not introduce any significant number of interface traps. Moreover, the fact that the value of the depletion capacitance is the same between the flat and the SiNW capacitors implies that the SiNWs in our system become fully depleted by the applied voltage at a value which is only -0.1V smaller than in the case of the flat capacitor.

In conclusion, we have developed and characterized a model system for the experimental extraction of SiNW MIS capacitor parameters, the knowledge of which is necessary for applications in memories, energy storage and sensor systems, logic etc.

ACKNOWLEDGMENT

This work was financially supported by the Greek national project "Establishing a multidisciplinary and effective innovation and entrepreneurship hub" (Project No 11928, 23-4-2015) and by LAAS-CNRS micro and nanotechnologies platform, member of the French RENATECH network.

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